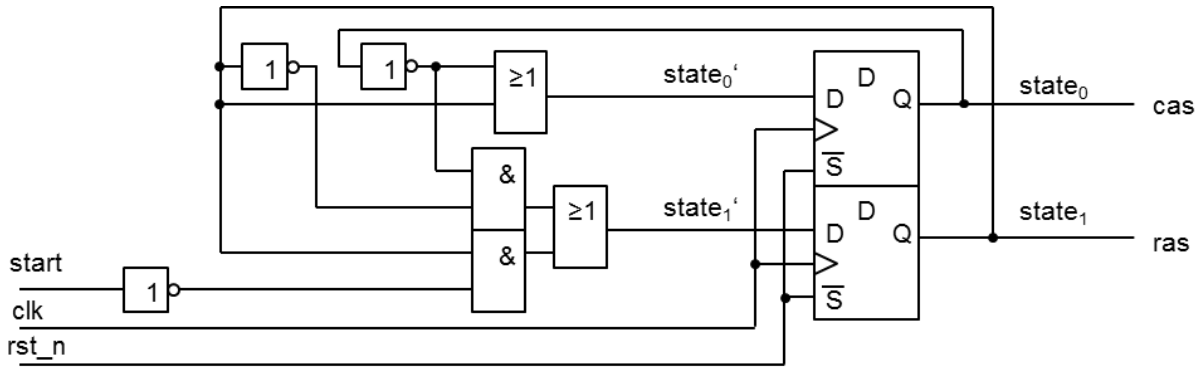
Praktikumsversuch 7: „Digitale Schaltungstechnik“ im Modul „Elektronik 2“

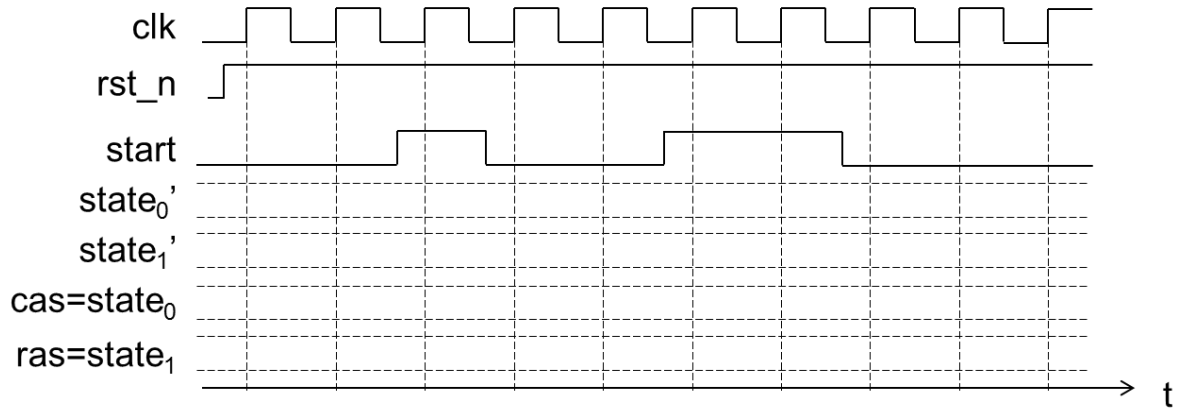
1 Vorbereitung

Die Aufgaben zur Versuchsvorbereitung sind von jedem Studierendem selbst als Hausaufgaben schriftlich auszuführen und dem gemeinsamen Protokoll der Versuchsgruppe beizufügen. Sie werden in die Bewertung des Versuches einbezogen. Ebenso zur Vorbereitung des Praktikums gehört, sich über **alle Versuchsaufgaben** zu informieren und diese, soweit das möglich ist, theoretisch vorzubereiten (Diagramme, Tabellen, Literatur). Jede Praktikumsgruppe fertigt ein Protokoll an, welches innerhalb von 2 Wochen abzugeben ist (**spätestens zu Semesterende**).

Aufgabe 1.1

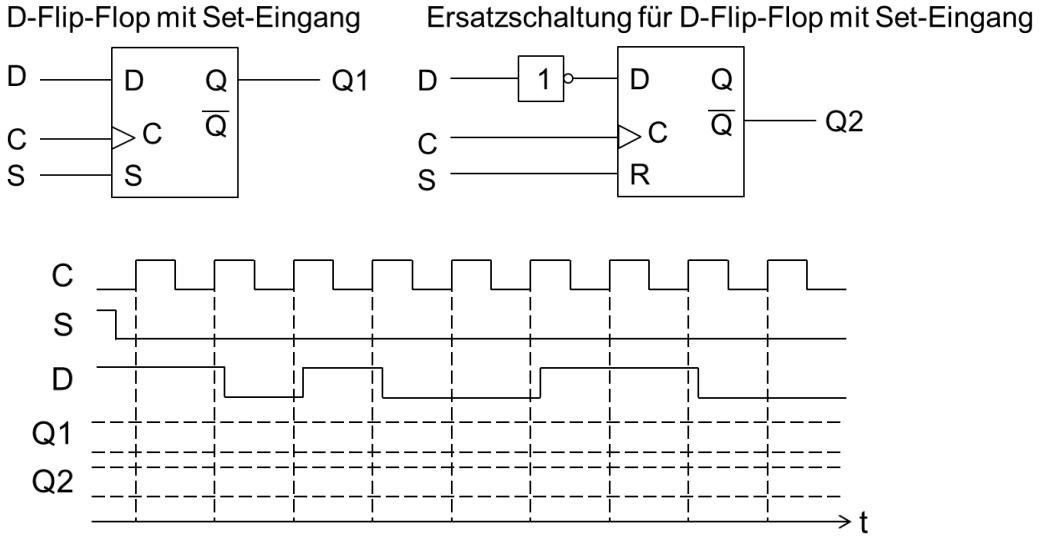
Geben Sie zur abgebildeten Schaltung den Signalverlauf für den angegebenen Signalverlauf an den Eingängen an!





Aufgabe 1.2

Angenommen, für eine Schaltung wird ein D-Flip-Flop mit high-aktivem Set-Eingang (Preset, PRE) benötigt. Zur Verfügung stehen aber lediglich D-Flip-Flop mit high-aktivem Reset-Eingang (Clear, CLR). Weisen Sie anhand der gegebenen Abfolge nach, dass die Ersatzschaltung sich genauso verhält, wie ein D-Flip-Flop mit Set-Eingang!



Aufgabe 1.3

Für Anzeigen haben sich in einigen Bereichen LED-Zeilen etabliert, bei denen die Anzahl der leuchtenden LEDs dem anzuzeigenden Wert entspricht, z. B. Lautstärkeanzeigen in Audio-Anlagen oder die untere Zeile in der Anzeige der Multimeter vom Typ Fluke 29/73/79/87 (Praktikum Analoge Schaltungstechnik). Diese Kodierung wird Thermometercode genannt. In der Aufgabe 3.2 soll eine Schaltung aufgebaut werden, mit der die Binär-Werte für 0…3 (2 Bit) mit 3 LEDs als Thermometercode visualisiert werden sollen.

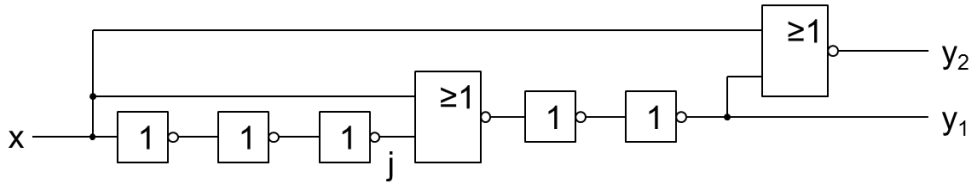
Erstellen Sie eine Wertetabelle des erwarteten Verhaltens (d. h. Kodierung Binär-nach-Thermometercode) der Schaltung anhand der booleschen Formeln!

Zahl	x_1	x_0	y_2	y_1	y_0
0					
1					
2					
3					

Erstellen Sie zu Aufgabe 3.2 (Thermometercode) einen Schaltplan! Verwenden Sie ausschließlich die auf dem Board zur Verfügung stehenden Gatter!

Aufgabe 1.4

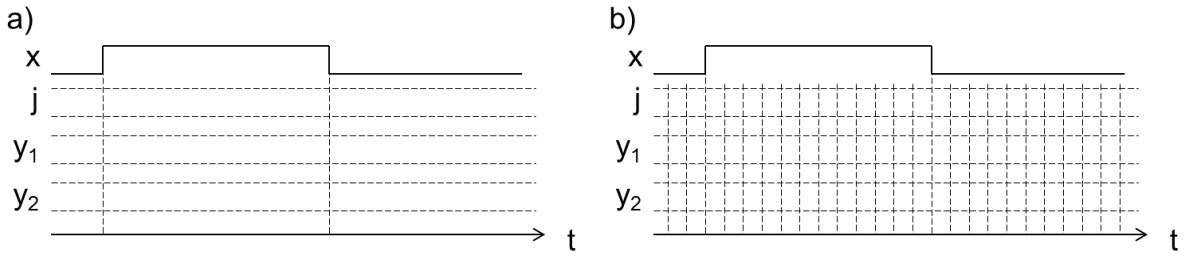
Stellen Sie die Wertetabelle für die angegebene Schaltung aus Aufgabe 3.3 (Hazards) auf!



x	j	y_1	y_2
0			
1			

Skizzieren Sie den Werteverlauf am Ausgang für ein periodisches Signal am Eingang!

a) Ideale Gatter ohne Verzögerungszeiten
b) Reale Gatter mit Verzögerungszeiten (alle Gatter haben gleiche Verzögerungszeiten)



Aufgabe 1.5

Zeichnen Sie zu jeder Schaltung, die im Praktikum aufgebaut wird (Abschnitte 2-4), ein Verdrahtungsschema (Vorlage S. 15)!

- Es ist sinnvoll, die Verdrahtung mehrfarbig zu zeichnen.
- Die Verdrahtung kann Luftlinie über die ICs gezeichnet werden.
- Das Verdrahtungsschema für die jeweilige Schaltung kann auf den benötigten Ausschnitt der Vorlage beschränkt werden. Dadurch kann der Ausschnitt vergrößert dargestellt werden.

Alternativ zum Verdrahtungsplan können Sie auch in jedem Schaltplan an jeden Gattereinund -ausgang die Nummer des entsprechenden Schaltkreispins notieren.

2 Elektrische Eigenschaften von CMOS-Invertern

Die Messungen werden an einem Schaltkreis 74HC04 mit je 6 Invertern (U_{DD} = 5V) vorgenommen.

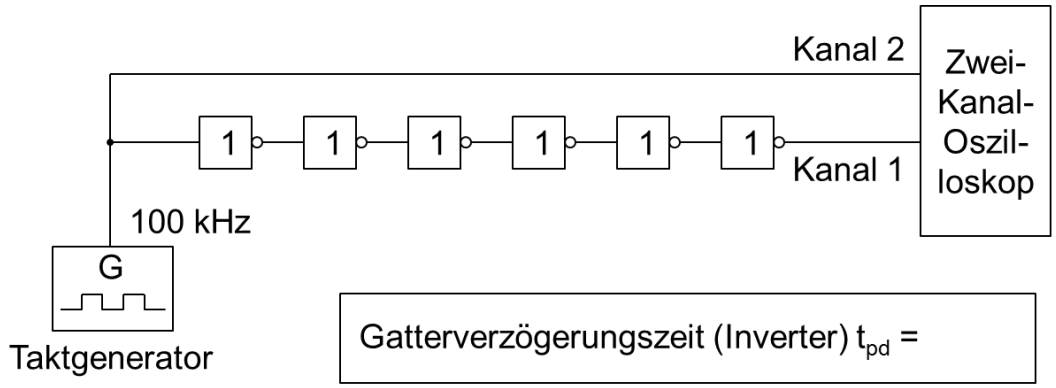
Aufgabe 2.1 Statisches Verhalten

a) Nehmen Sie die Spannungs-Übertragungs-Kennlinie (SÜK) eines unbelasteten CMOS-Gatters auf und stellen Sie diese in einem Diagramm dar! Nutzen Sie das Potentiometer „G-“ auf dem Board!
b) Messen Sie die Stromaufnahme I_{DD} des ICs 74HC04 in Abhängigkeit von U_{in} (Messgerät in Betriebsspannungszufuhr von IC1) und stellen Sie diese in einem Diagramm dar! Verbinden Sie dazu alle Inverter-Eingänge miteinander!
c) Bestimmen Sie R_{DSon} des p-Kanal-MOSFET am Inverter-Ausgang! Belasten Sie dazu den Ausgang bei U_{in}=0V durch eine Widerstandsdekade so, dass die Ausgangsspannung um ca. 0,2 V abfällt.
d) Bestimmen Sie aus den Messwerten die statischen Störspannungsabstände S_H und S_L!

Aufgabe 2.2 Dynamisches Verhalten

a) Bestimmen Sie die Anstiegs- und Abfallzeit eines CMOS-Inverters des 74HC04 (unbelasteter Ausgang)
   Hinweis zur Messung: Oszilloskop auf 1V/div einstellen und mit Cursor Zeiten bestimmen
b) Bestimmen Sie die Anstiegszeit eines CMOS-Inverters des 74HC04
   (1) Ausgang mit Fan-out = 5 (Eingänge der anderen 5 Inverter des 74HC04)
   (2) Ausgang mit Fan-out = 13 (Eingänge der anderen 5 Inverter des 74HC04 und 8 Eingänge des 74HC02)!
   Stellen Sie die Werte in einem Diagramm dar (Anstiegszeit als Funktion des Fan-Outs)!
c) Bestimmen Sie die Anstiegszeit eines CMOS-Inverters des 74HC04 bei einer Belastung durch eine Kapazität 68 pF!
   Wie groß ist in etwa in Kapazität eines Gattereingangs des 74HC04/74HC02 (Abschätzung auf Basis der Ergebnisse von a) und b))? Vergleichen Sie den Wert mit den Angaben im Datenblatt!
d) Schalten Sie 6 Inverter (74HC04) in Reihe und ermitteln Sie mit Hilfe des Oszilloskops die mittleren Gatterlaufzeiten pro Gatter!

Hinweis zur Durchführung: Nutzen Sie die Möglichkeiten der Triggerung des Oszilloskops auf die steigende oder fallende Flanke zur Visualisierung beider Flanken! Verwenden Sie DC-Kopplung!



Aufgabe 2.3 Verlustleistung

Bestimmen Sie die mittlere Stromaufnahme und die mittlere Verlustleistung des Schaltkreises 74HC04 (Funktion: 6 Inverter in Reihe) in Abhängigkeit von der Schaltfrequenz (f_{Gen} = 1 kHz, 10 kHz und 100 kHz)! (Darstellung in Diagramm)

Hinweis zur Durchführung: Messgerät in Betriebsspannungszuführung von IC1.

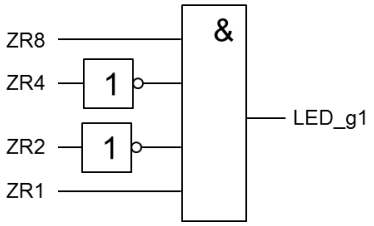
3 Kombinatorische Schaltungen

Alle Messgeräte sind vom Board zu entfernen.

Aufgabe 3.1 Zahlenschloss (kombinatorisch)

Bauen Sie die folgende Schaltung eines einfachen Zahlenschlosses auf! Die Eingänge sind mit der Zifferneingabe rechts zu verbinden, der Ausgang mit der LED_g1.

Realisieren Sie das AND-Gatter (4 Eingänge, AND4) durch Kaskadierung aus AND-Gattern mit 2 Eingängen (AND2)!



Für welche Eingabe öffnet sich das Schloss (= 1 am Ausgang)?

Ändern Sie die Schaltung, so dass sich das Schloss bei einer selbst-gewählten Zahl öffnet! (Zahl und Schaltung im Protokoll)

Aufgabe 3.2 Thermometer-Code

Bauen Sie eine Schaltung entsprechend der gegebenen Booleschen Formeln bzw. der Schaltung gemäß Aufgabe 1.3 auf und bestimmen Sie ihr Verhalten in Form einer Wertetabelle!

Die Eingänge x_i sind mit der Zifferneingabe rechts zu verbinden (x_0 = ZR1, x_1 = ZR2), die Ausgänge mit den LEDs (y_0=LED_g4, y_1=LED_g3, y_2=LED_g2).

Verwenden Sie Schaltkreise 74HC08 (4AND2), 74HC02 (4NOR2) und 74HC04 (6INV) und realisieren Sie die ODER-Verknüpfung durch NOR-Gatter und Inverter!

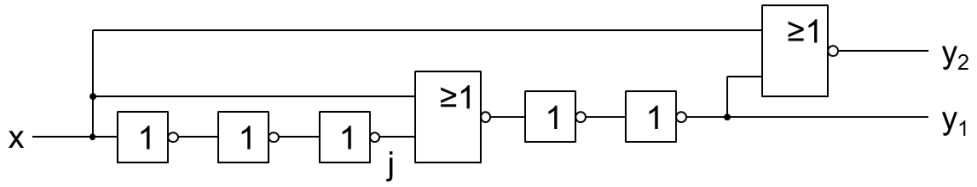
LED_g4: $y_0 = x_1 \vee x_0$
LED_g3: $y_1 = x_1$
LED_g2: $y_2 = x_1 \wedge x_0$

Hinweis zum Aufbau: Prüfen Sie vor Beginn des Aufbaus, dass die Verbindungen aller ICs zu Masse und Betriebsspannung vorhanden sind!

Zahl	$\mathbf{x_1}$	$\mathbf{x_0}$	$\mathbf{y_2}$	$\mathbf{y_1}$	$\mathbf{y_0}$
0					
1					
2					
3					

Aufgabe 3.3 Hazards

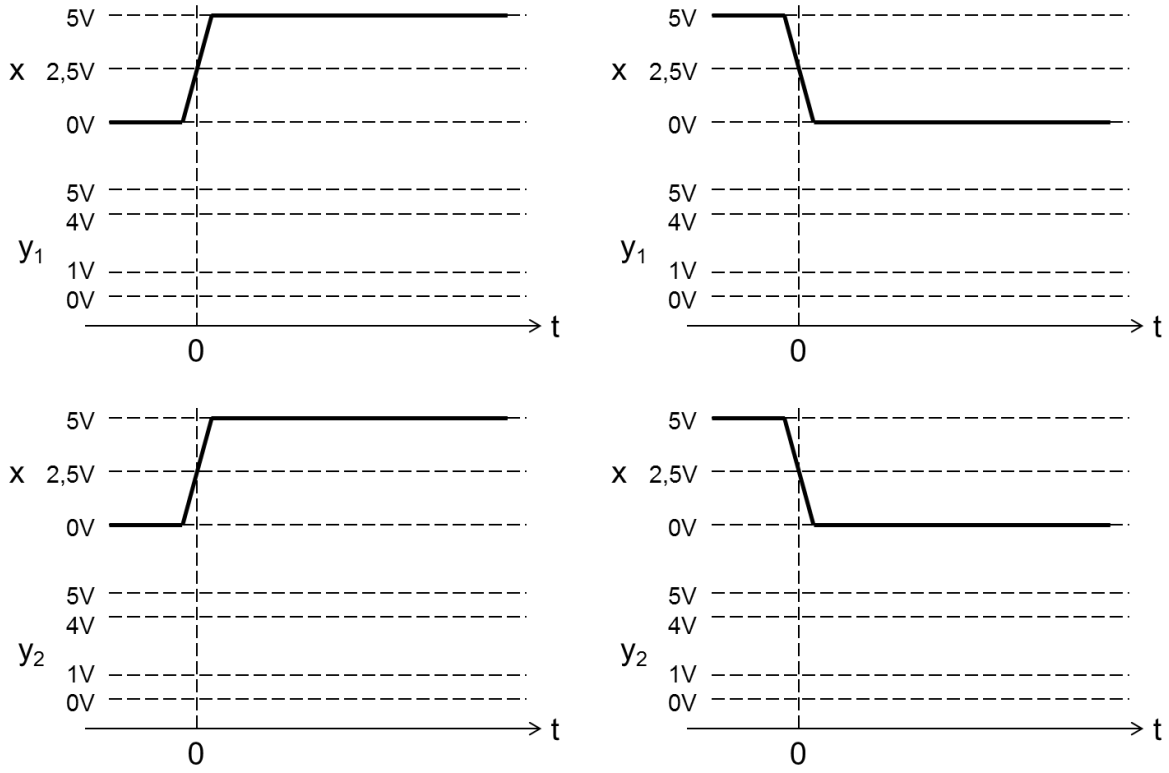
Bauen Sie die folgende Schaltung auf!



Bestimmen Sie das statische Verhalten der Schaltung! (Eingang x mit LH1 und Ausgänge mit LEDs verbinden)

x	y_1	y_2
0		
1		

Bestimmen Sie das dynamische Verhalten der Schaltung bei Flanken an x! Stellen Sie dazu das Eingangs- und Ausgangssignal am Oszilloskop dar! Skizzieren Sie den Werteverlauf einschließlich Beschriftung der t-Achse! Der Eingang x ist mit dem Generator (100 kHz) zu verbinden.



4 Sequenzielle Schaltungen

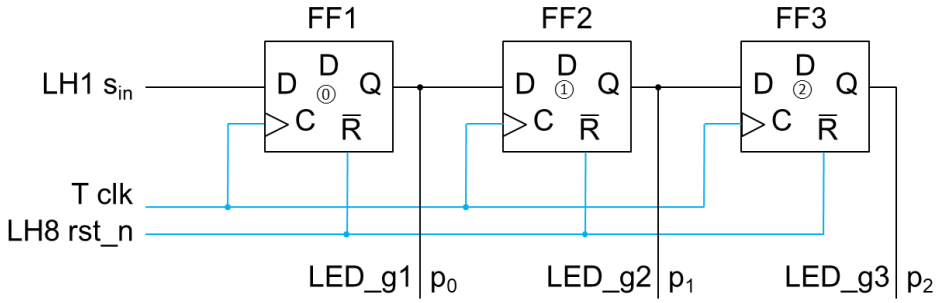
Allgemeine Hinweise für Flip-Flops:

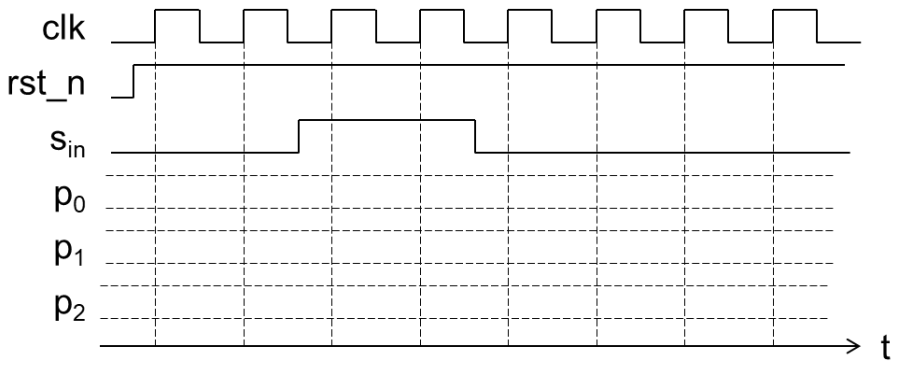
- Der Reset-Eingang R des verwendeten ICs 74HC175 wird im Datenblatt mit CLR bezeichnet und ist low-aktiv. Daher ist der Schaltungs-Eingang rst_n auch low-aktiv.
- Die Flip-Flops besitzen einen Ausgang /Q. Dieser entspricht der Negation des Ausgangs Q und kann genutzt werden, um Verdrahtungsaufwand zu sparen, wenn der Ausgang Q in der Schaltung über einen Inverter negiert wird.

Aufgabe 4.1 Schieberegister

a) Bauen Sie das folgende Schieberegister auf! Protokollieren Sie das Verhalten im Diagramm!

Hinweis zur Durchführung: Verbinden Sie zuerst die Takt- und Reset-Leitung und die LEDs mit den Flip-Flops! Nutzen Sie die Flip-Flops im 74HC175 entsprechend der **angegebenen Nummern in den Kreisen**!



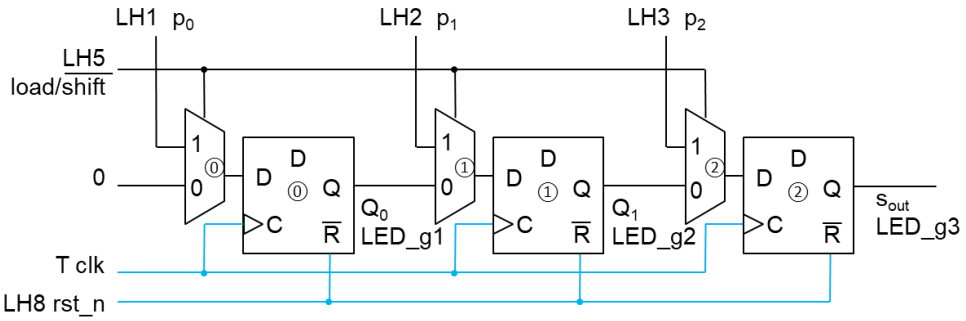


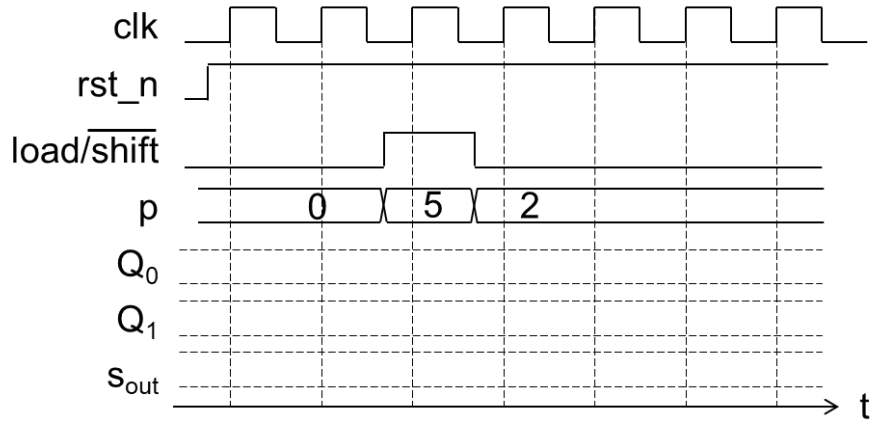
Beschreiben Sie das Verhalten am Ausgang p_2 bezüglich des Eingangs s_{in}!

Beschreiben Sie den Wert am Ausgangsvektor p = (p_2, p_1, p_0) bezüglich des Eingangs s_{in} verbal!

b) Bauen Sie das folgende Schieberegister auf! Protokollieren Sie das Verhalten im Diagramm!

Hinweis: Verbinden Sie zuerst die Takt- und Reset-Leitung und die LEDs mit den Flip-Flops! Nutzen Sie die Flip-Flops im 74HC175 und Multiplexer im 74HC157 entsprechend der **angegebenen Nummern in den Kreisen**! Beachten Sie den **Anschluss G des Multiplexer-ICs**, welcher mit L verbunden werden muss!

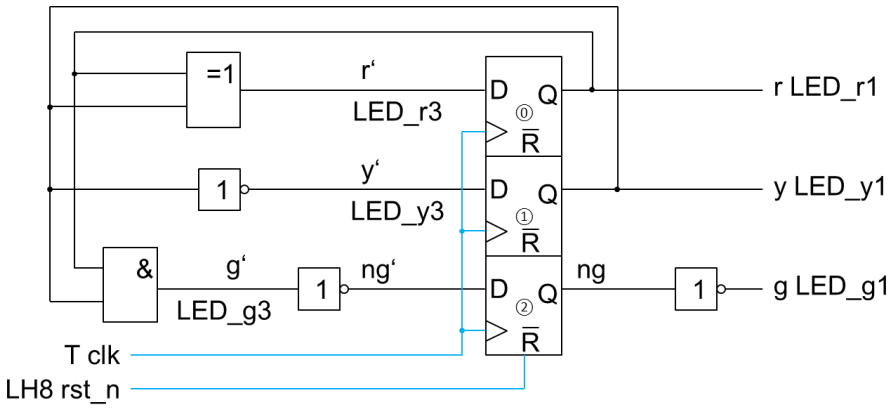


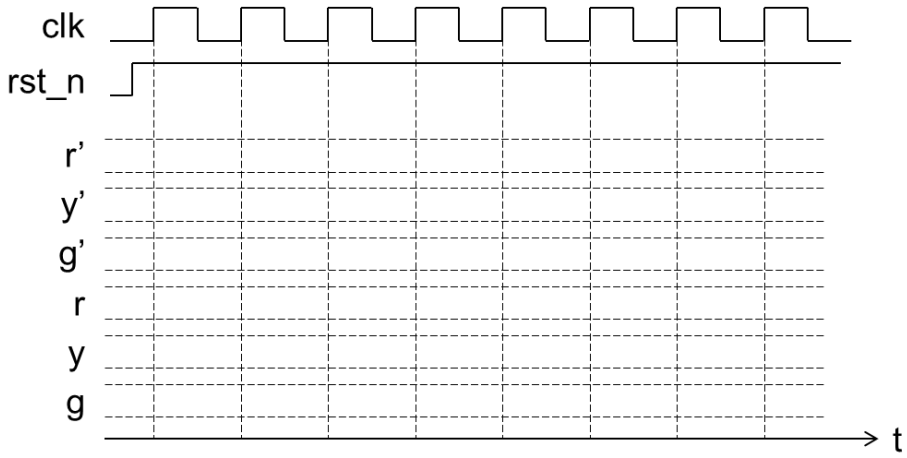


Beschreiben Sie den Wert am Ausgang s_{out} bezüglich des Eingangsvektor p = (p_2, p_1, p_0) verbal!

Aufgabe 4.2 Ampel

Bauen Sie die folgende Schaltung einer Ampel auf! Nutzen Sie ggf. anstelle der Inverter die negierten Ausgänge (/Q) der Flip-Flops! Protokollieren Sie das Verhalten (Ausgabe/Zustand und Folgezustand) im Diagramm!



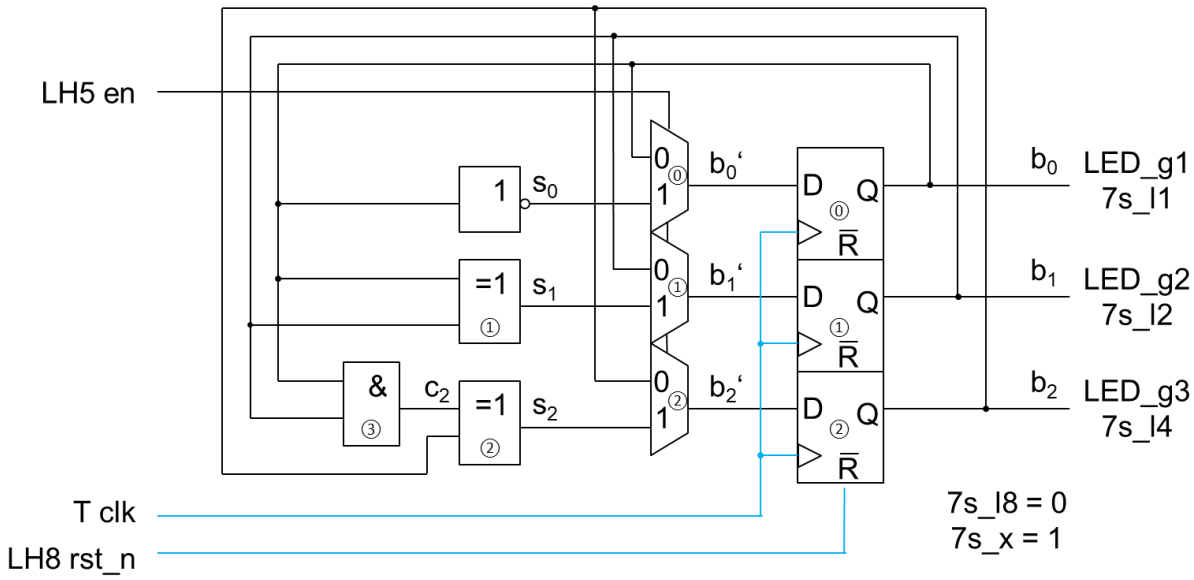


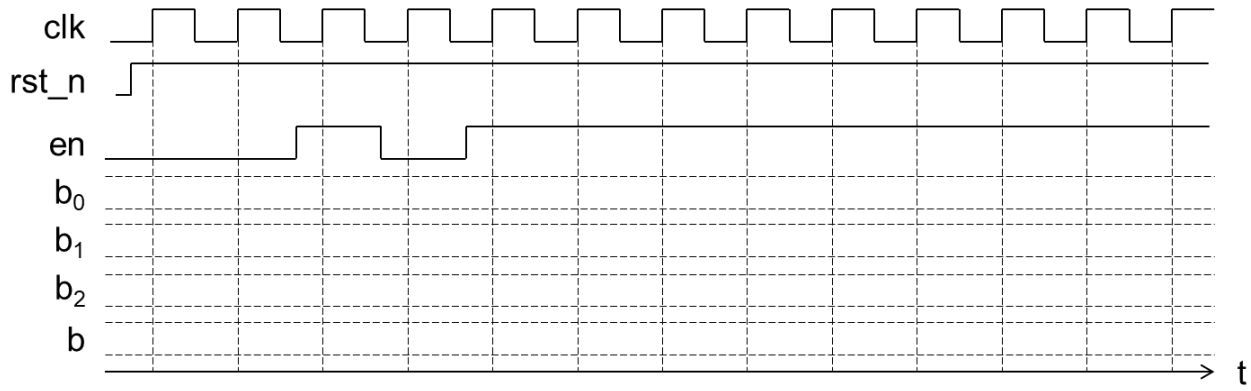
Aufgabe 4.3 Zähler

Bauen Sie die folgende Schaltung auf! Protokollieren Sie das Verhalten am Vektor b = (b_2, b_1, b_0) im Diagramm! (b als Dezimalzahl)

Hinweise:

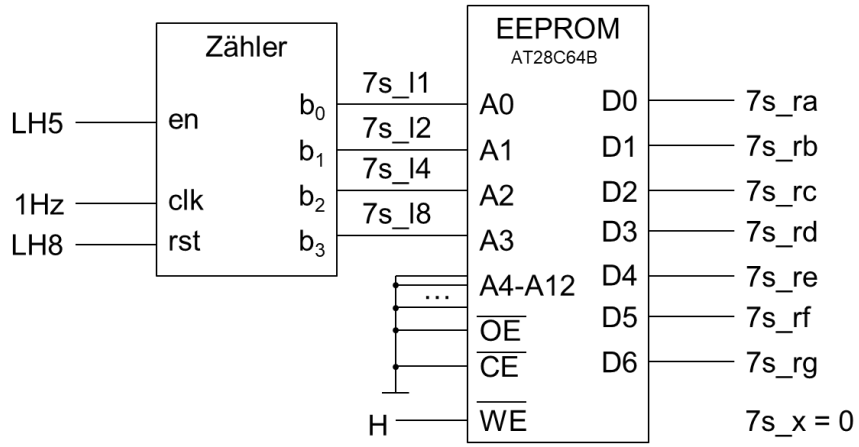
- Verbinden Sie zuerst die Takt- und Reset-Leitung und die LEDs und 7-Segment-Anzeigen mit den Flip-Flops! Nutzen Sie die Flip-Flops im 74HC175 und Multiplexer im 74HC157 entsprechend der **angegebenen Nummern in den Kreisen**!
- Beachten Sie den **Anschluss G des Multiplexer-ICs**, welcher mit L verbunden werden muss!
- Nach erfolgreichem Funktionstest kann der Eingang clk mit dem Taktgenerator (0,1 Hz) verbunden werden.





Aufgabe 4.4 Speicher

Verbinden Sie den Ausgang b des Zählers aus Aufgabe 4.3 mit dem Adress-Eingang des EEPROMs AT28C64B (IC11)! Lassen Sie den Zähler von 0 bis 7 laufen und protokollieren Sie den Inhalt des EEPROMs!

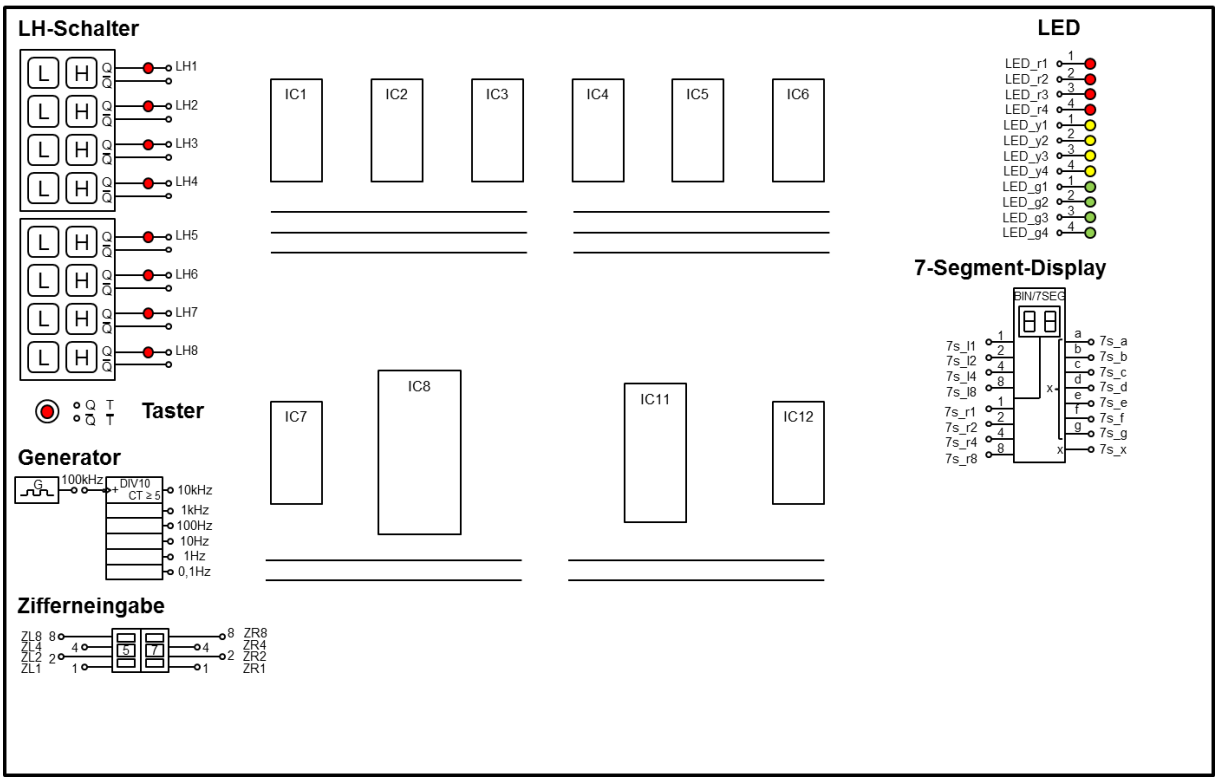


ROM-Beschriftung:

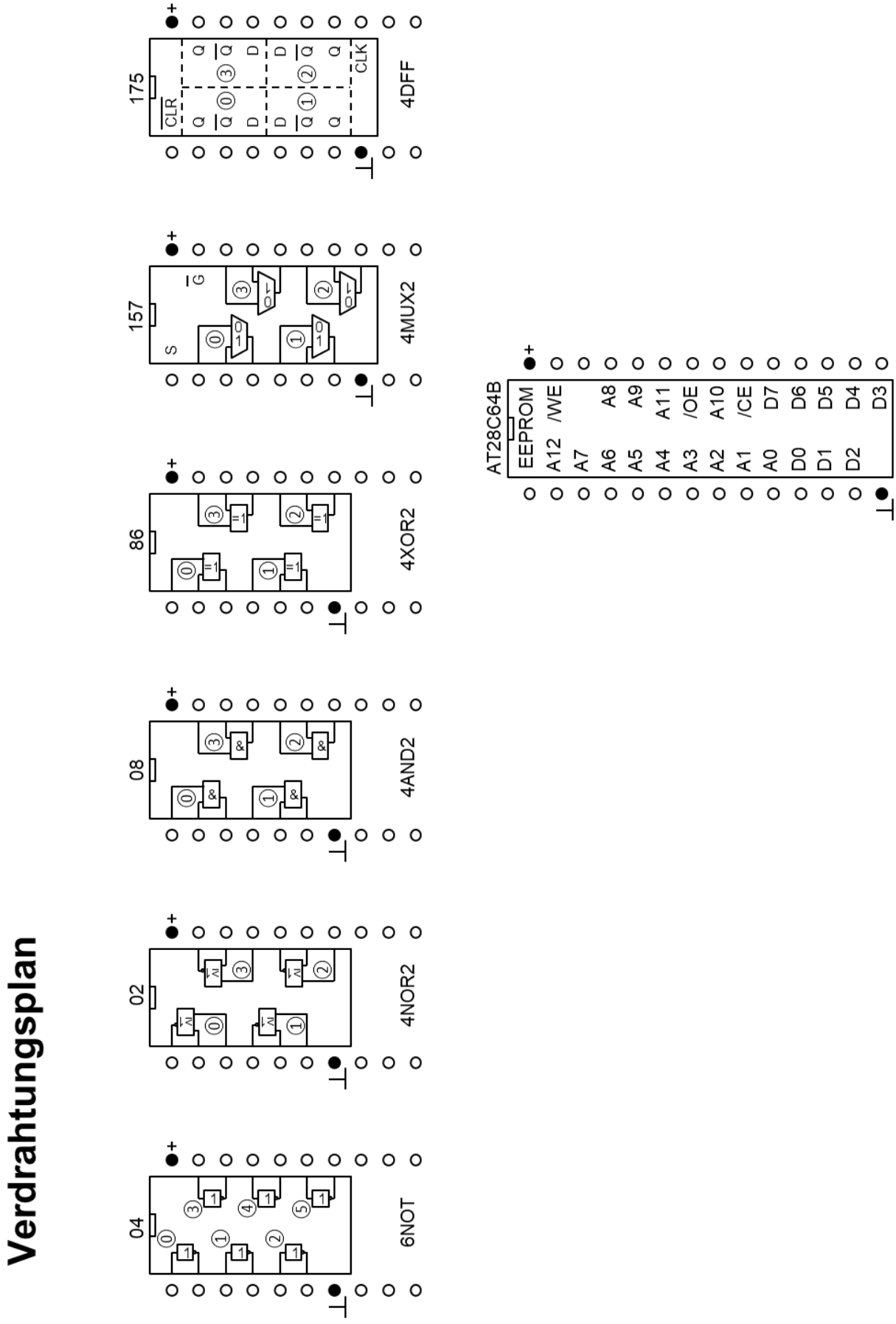
Adresse (hex)	0	1	2	3	4	5	6	7
Anzeige								

5 Anhang

Digi IC Board



Verdrahtungsplan



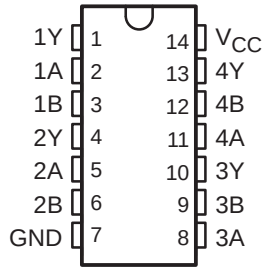
Excerpt

SN54HC02, SN74HC02
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

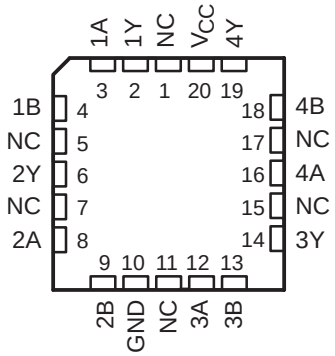
SCLS076E – DECEMBER 1982 – REVISED AUGUST 2003

- **Wide Operating Voltage Range of 2 V to 6 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 20-μA Max I_{CC}**
- **Typical t_{pd} = 8 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**

SN54HC02 . . . J OR W PACKAGE
SN74HC02 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC02 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The ’HC02 devices contain four independent 2-input NOR gates. They perform the Boolean function $Y = \overline{A + B}$ or $Y = \overline{A} \bullet \overline{B}$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74HC02N	SN74HC02N
	SOIC – D	Tube of 50	SN74HC02D	HC02
		Reel of 2500	SN74HC02DR	
		Reel of 250	SN74HC02DT	
	SOP – NS	Reel of 2000	SN74HC02NSR	HC02
	SSOP – DB	Reel of 2000	SN74HC02DBR	HC02
	TSSOP – PW	Tube of 90	SN74HC02PW	HC02
		Reel of 2000	SN74HC02PWR	
		Reel of 250	SN74HC02PWT	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC02J	SNJ54HC02J
	CFP – W	Tube of 150	SNJ54HC02W	SNJ54HC02W
	LCCC – FK	Tube of 55	SNJ54HC02FK	SNJ54HC02FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
PW package . . . . . 113°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54HC02			SN74HC02			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5			0.5	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 6 V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time	V_{CC} = 2 V			1000			1000	ns
		V_{CC} = 4.5 V			500			500	
		V_{CC} = 6 V			400			400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

HEX INVERTERS

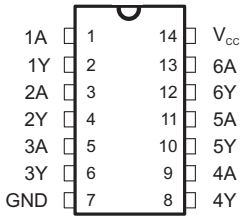
Excerpt

Check for Samples: SN54HC04, SN74HC04

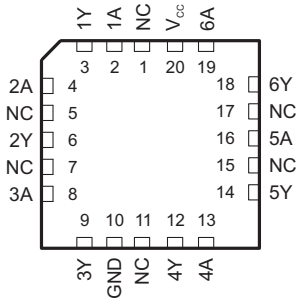
FEATURES

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20-μA Max I_{CC}
- Typical t_{pd} = 8 ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1 μA Max

SN54HC04...J OR W PACKAGE
SN74HC04...D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC04...FK PACKAGE
(TOP VIEW)



NC – No internal connection

DESCRIPTION/ORDERING INFORMATION

The ’HC04 devices contain six independent inverters. They perform the Boolean function Y = $\overline{A}$ in positive logic.

ORDERING INFORMATION

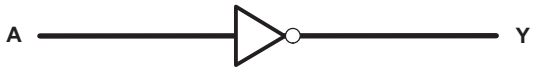
T_A	PACKAGE(1)		ODERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Reel of 1000	SN74HC04N	SN74HC04N
	SOIC – D	Reel of 1000	SN74HC04DE4	HC04
		Reel of 2500	SN74HC04DRG3	
		Tube of 250	SN74HC04DT	
	SOP – NS	Reel of 2000	SN74HC04NSR	HC04
			SN74HC04NSRG4	
	SSOP – DB	Reel of 2000	SN74HC04DBR	HC04
			SN74HC04DBRE4	
	TSSOP – PW	Tube of 90	SN74HC04PW	HC04
		Reel of 2000	SN74HC04PWR	
		Tube of 250	SN74HC04PWT	
–55°C to 125°C	CDIP – J	Reel of 1000	SNJ54HC04J	
	CFP – W	Reel of 900	SNJ54HC04W	
	LCCC –FK	Reel of 2200	SNJ54HC04FK	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Table 1. FUNCTION TABLE (EACH INVERTER)

INPUT A	OUTPUT Y
H	L
L	H

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance(3)	D package		86	°C/W
		N package		80	
		NS package		76	
		PW package		113	
T_{stg}	Storage temperature range		–60	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

			SN54HC04			SN74HC04			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5			0.5	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 6 V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2 V			1000			1000	ns
		V_{CC} = 4.5 V			500			500	
		V_{CC} = 6 V			400			400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC04		SN74HC04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0		6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

Switching Characteristics

over operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

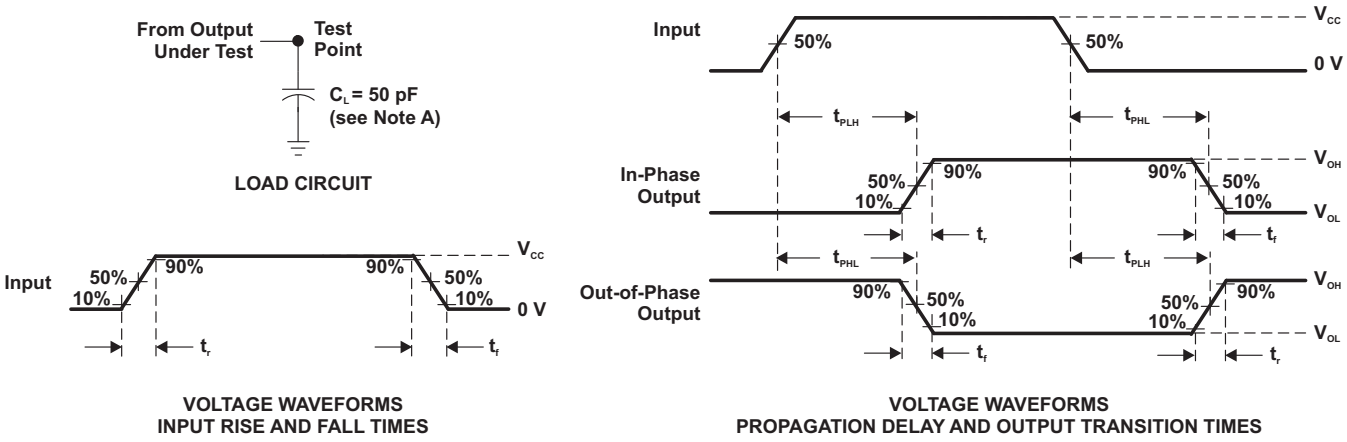
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC04		SN74HC04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		45	95		125		120	ns
			4.5 V		9	19		29		24	
			6 V		8	16		25		20	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	No load	20	pF

PARAMETER MEASURMENT INFORMATION



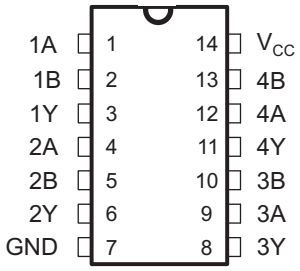
NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_o = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

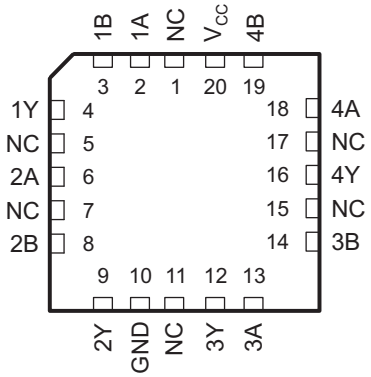
FEATURES

- **Wide Operating Voltage Range of 2 V to 6 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 20-μA Max I_{CC}**
- **Typical t_{pd} = 8 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**

SN54HC04...J OR W PACKAGE
SN74HC04...D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC04...FK PACKAGE
(TOP VIEW)



NC – No internal connection

DESCRIPTION/ORDERING INFORMATION

The 'HC08 devices contain four independent 2-input AND gates. They perform the Boolean function $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

ORDERING INFORMATION

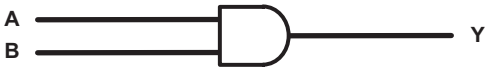
T_A	PACKAGE(1)		ODERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Reel of 1000	SN74HC08N	SN74HC08N
	SOIC – D	Reel of 1000	SN74HC08DE4	HC08
		Reel of 2500	SN74HC08DR	
		Tube of 250	SN74HC08DT	
	SOP – NS	Reel of 2000	SN74HC08NSR	HC08
			SN74HC08NSRG4	
	SSOP – DB	Reel of 2000	SN74HC08DBR	HC08
			SN74HC08DBRE4	
	TSSOP – PW	Tube of 90	SN74HC08PW	HC08
		Reel of 2000	SN74HC08PWR	
		Tube of 250	SN74HC08PWT	
–55°C to 125°C	CDIP – J	Reel of 1000	SNJ54HC08J	SNJ54HC08J
	CFP – W	Reel of 900	SNJ54HC08W	SNJ54HC08W
	LCCC –FK	Reel of 2200	SNJ54HC08FK	SNJ54HC08JFK

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (EACH INVERTER)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance(3)	D package		86	°C/W
		DB package		96	
		N package		80	
		NS package		76	
		PW package		113	
T_{stg}	Storage temperature range		–60	150	°C

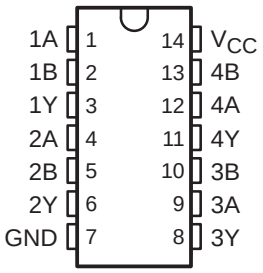
(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

SN54HC86, SN74HC86
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

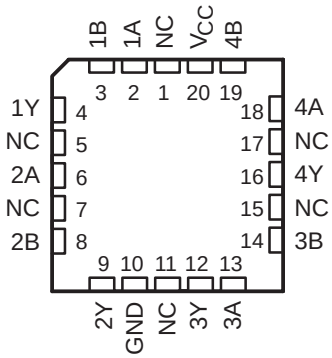
SCLS100E – DECEMBER 1982 – REVISED AUGUST 2003

- **Wide Operating Voltage Range of 2 V to 6 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 20-μA Max I_{CC}**
- **Typical t_{pd} = 10 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**
- **True Logic**

SN54HC86 . . . J OR W PACKAGE
SN74HC86 . . . D, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC86 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These devices contain four independent 2-input exclusive-OR gates. They perform the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74HC86N	SN74HC86N
	SOIC – D	Tube of 50	SN74HC86D	HC86
		Reel of 2500	SN74HC86DR	
		Reel of 250	SN74HC86DT	
	SOP – NS	Reel of 2000	SN74HC86NSR	HC86
	TSSOP – PW	Tube of 90	SN74HC86PW	HC86
		Reel of 2000	SN74HC86PWR	
		Reel of 250	SN74HC86PWT	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC86J	SNJ54HC86J
	CFP – W	Tube of 150	SNJ54HC86W	SNJ54HC86W
	LCCC – FK	Tube of 55	SNJ54HC86FK	SNJ54HC86FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

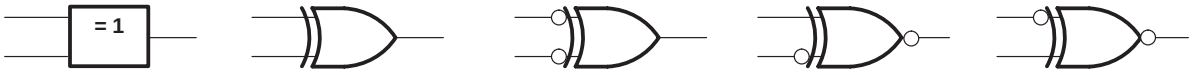
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

exclusive-OR logic

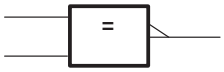
An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

Exclusive OR



These are five equivalent exclusive-OR symbols valid for an ’HC86 gate in positive logic; negation may be shown at any two ports.

Logic Identity Element

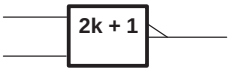


The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

Even-Parity Element

The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

Odd-Parity Element



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 86°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
PW package . . . . . 113°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

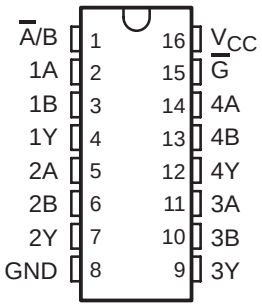
Excerpt

SN54HC157, SN74HC157
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

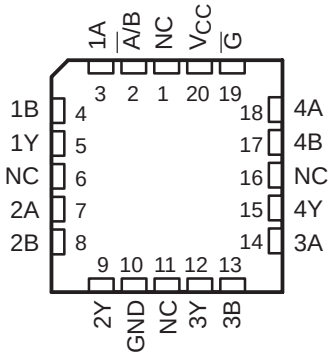
SCLS113D − DECEMBER 1982 − REVISED SEPTEMBER 2003

- **Wide Operating Voltage Range of 2 V to 6 V**
- **Outputs Can Drive Up To 15 LSTTL Loads**
- **Low Power Consumption, 80-μA Max I_{CC}**
- **Typical t_{pd} = 11 ns**
- **±6-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**

SN54HC157 . . . J OR W PACKAGE
SN74HC157 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC157 . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

These data selectors/multiplexers contain inverters and drivers to supply full data selection to the four output gates. A separate strobe ($\overline{G}$) input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The ’HC157 devices present true data.

ORDERING INFORMATION

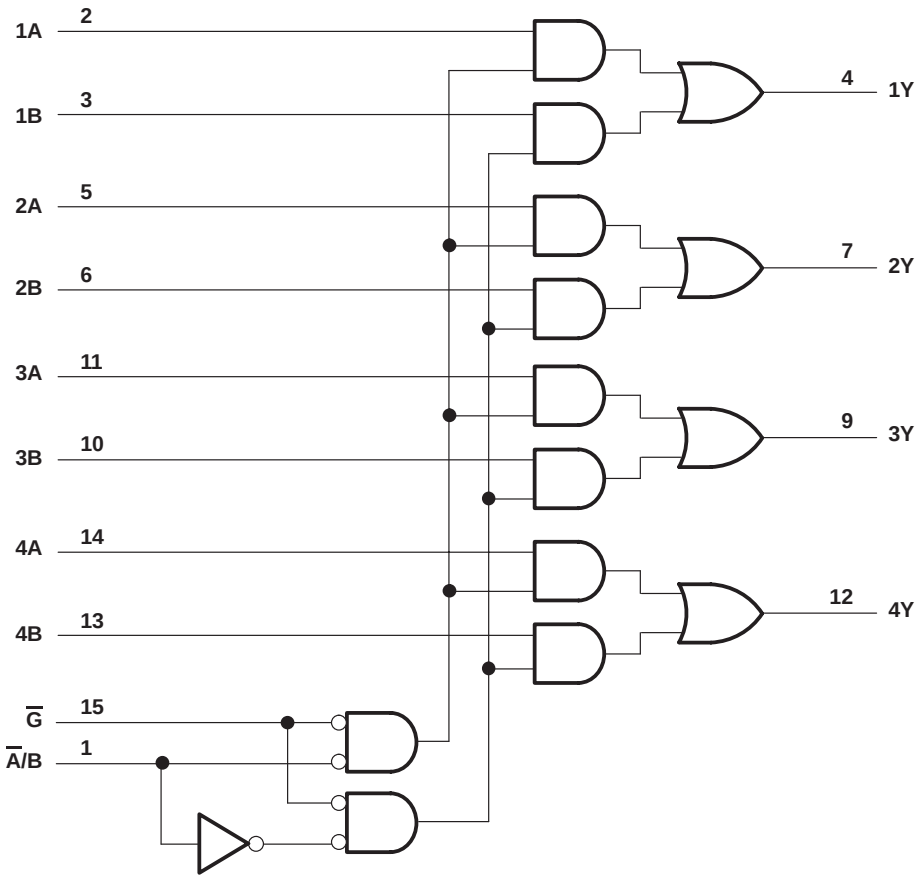
T_A	PACKAGE†	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP − N	Tube of 25	SN74HC157N	SN74HC157N
	SOIC − D	Tube of 40	SN74HC157D	HC157
		Reel of 2500	SN74HC157DR	
		Reel of 250	SN74HC157DT	
	SOP − NS	Reel of 2000	SN74HC157NSR	HC157
	SSOP − DB	Reel of 2000	SN74HC157DBR	HC157
	TSSOP − PW	Tube of 90	SN74HC157PW	HC157
		Reel of 2000	SN74HC157PWR	
		Reel of 250	SN74HC157PWT	
−55°C to 125°C	CDIP − J	Tube of 25	SNJ54HC157J	SNJ54HC157J
	CFP − W	Tube of 150	SNJ54HC157W	SNJ54HC157W
	LCCC − FK	Tube of 55	SNJ54HC157FK	SNJ54HC157FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{G}$	SELECT $\overline{A}$/B	DATA		Y
		A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

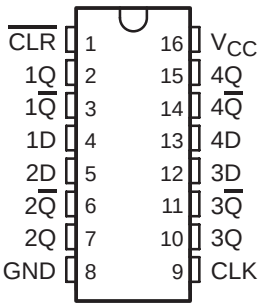
Excerpt

SN54HC175, SN74HC175
QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

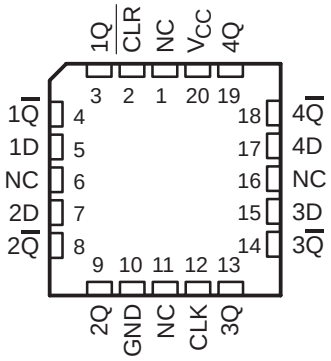
SCLS299D − JANUARY 1996 − REVISED SEPTEMBER 2003

- **Wide Operating Voltage Range of 2 V to 6 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 80-μA Max I_{CC}**
- **Contain Four Flip-Flops With Double-Rail Outputs**
- **Typical t_{pd} = 13 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**

SN54HC175 . . . J OR W PACKAGE
SN74HC175 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC175 . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

These positive-edge-triggered D-type flip-flops have a direct clear ($\overline{CLR}$) input. The ’HC175 devices feature complementary outputs from each flip-flop.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP − N	Tube of 25	SN74HC175N	SN74HC175N
	SOIC − D	Tube of 40	SN74HC175D	HC175
		Reel of 2500	SN74HC175DR	
		Reel of 250	SN74HC175DT	
	SOP − NS	Reel of 2000	SN74HC175NSR	HC175
	SSOP − DB	Reel of 2000	SN74HC175DBR	HC175
	TSSOP − PW	Tube of 90	SN74HC175PW	HC175
		Reel of 2000	SN74HC175PWR	
		Reel of 250	SN74HC175PWT	
−55°C to 125°C	CDIP − J	Tube of 25	SNJ54HC175J	SNJ54HC175J
	CFP − W	Tube of 150	SNJ54HC175W	SNJ54HC175W
	LCCC − FK	Tube of 55	SNJ54HC175FK	SNJ54HC175FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

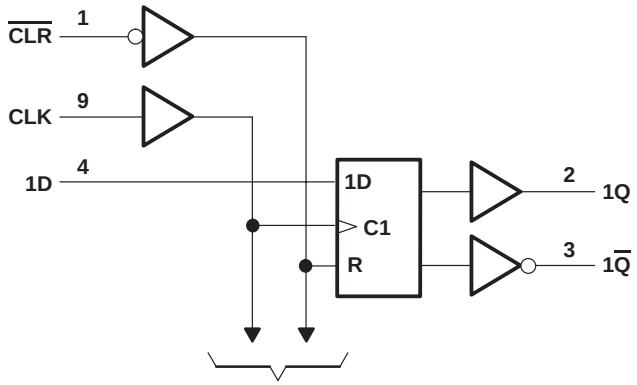
description/ordering information (continued)

Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not related directly to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUTS	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 73°C/W
DB package . . . . . 67°C/W
N package . . . . . 82°C/W
NS package . . . . . 64°C/W
PW package . . . . . 108°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

Features

- Fast Read Access Time – 150 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64 Bytes
- Fast Write Cycle Times
  - Page Write Cycle Time: 10 ms Maximum (Standard)
    2 ms Maximum (Option – Ref. AT28HC64BF Datasheet)
  - 1 to 64-byte Page Write Operation
- Low Power Dissipation
  - 40 mA Active Current
  - 100 µA CMOS Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling and Toggle Bit for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 100,000 Cycles
  - Data Retention: 10 Years
- Single 5V ±10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-wide Pinout
- Industrial Temperature Ranges
- Green (Pb/Halide-free) Packaging Option Only

64K (8K x 8) Parallel EEPROM with Page Write and Software Data Protection

AT28C64B

Excerpt

1. Description

The AT28C64B is a high-performance electrically-erasable and programmable read-only memory (EEPROM). Its 64K of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 220 mW. When the device is deselected, the CMOS standby current is less than 100 µA.

The AT28C64B is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ POLLING of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

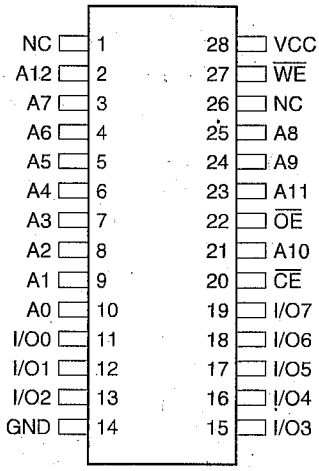
Atmel's AT28C64B has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.

0270L–PEEPR–2/09

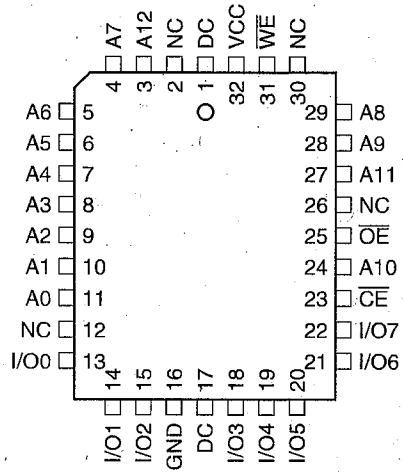
2. Pin Configurations

Pin Name	Function
A0 - A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

2.1 28-lead PDIP, 28-lead SOIC Top View

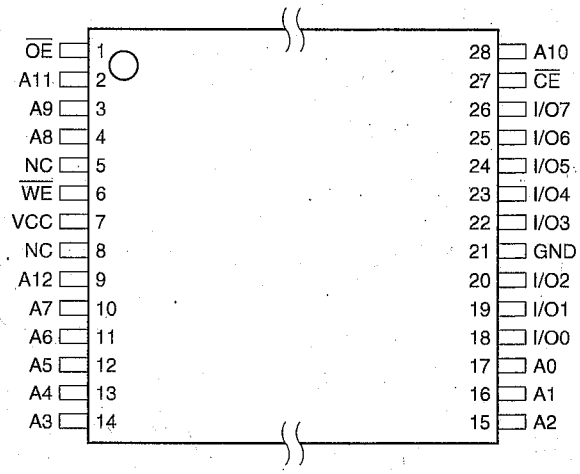


2.2 32-lead PLCC Top View

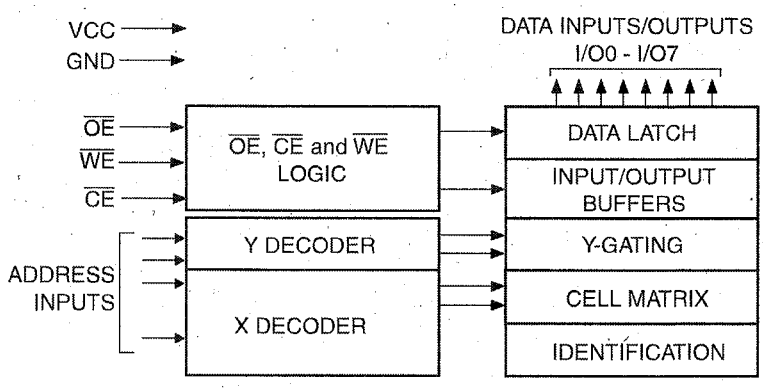


Note: PLCC package pins 1 and 17 are Don't Connect.

2.3 28-lead TSOP Top View



3. Block Diagram



4. Device Operation

4.1 Read

The AT28C64B is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high-impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention in their systems.

4.2 Byte Write

A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

4.3 Page Write

The page write operation of the AT28C64B allows 1 to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; after the first byte is written, it can then be followed by 1 to 63 additional bytes. Each successive byte must be loaded within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded, the AT28C64B will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 to A12 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A6 to A12 must be the same.

The A0 to A5 inputs specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

5. DC and AC Operating Range

	AT28C64B-15
Operating Temperature (Case)	-40°C - 85°C
V_{CC} Power Supply	5V ±10%

6. Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. See "AC Write Waveforms" on page 8.
3. V_H = 12.0V ±0.5V.

7. Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

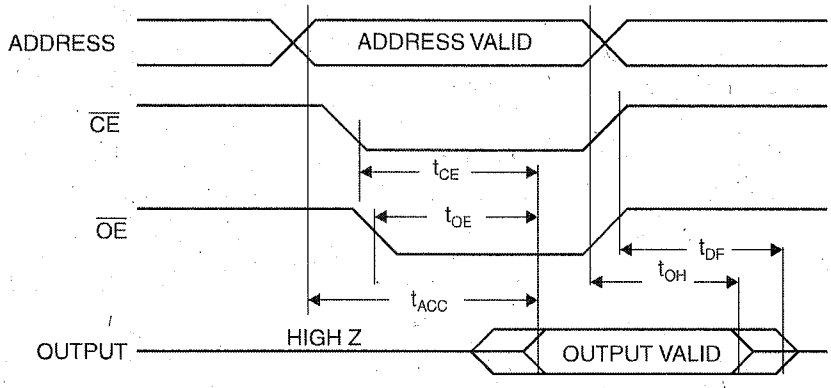
8. DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V		100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V		2	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		40	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.40	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

9. AC Read Characteristics

Symbol	Parameter	AT28C64B-15		Units
		Min	Max	
t_{ACC}	Address to Output Delay		150	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		150	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	70	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		ns

10. AC Read Waveforms[1][2][3][4]



Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.