Investigation of advanced FDSOI CMOS devices for analog/mixed signal applications

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***Abstract*— A comparison of CMOS devices with best in class noise behavior and low power consumption for analog/mixed signal applications has been achieved by extensive TCAD simulations. The intrinsic gain g_m/I_D of FDSOI transistors was optimized by several process adjustments. An advanced bulk device with improved noise behavior was used as a reference and different bias conditions were simulated. With certain layer optimizations the g_m/I_D was improved by 50% in the low power regime. An additional improvement up to 50% has been achieved by biasing the FDSOI device in double gate mode (DGM).**

Keywords-FDSOI; CMOS; Sentaurus TCAD; DGM; g_m/I_D

I. INTRODUCTION

The FDSOI transistor can be quite advantageous for analog/mixed signal applications and upcoming IoT devices where low power consumption and high intrinsic gain are equally important. This is inherently achieved by the low parasitic elements as well as the back gate controllability [1], [2].

A common example for analog and mixed signal applications is a read-out circuit comparator. So far, common bulk devices are used until the device scaling boosted the impact of low-frequency noise. The optimizations of the bulk devices are mainly done by so-called buried channel (BC) implantations were the noise performance could be improved [3].

On the other hand, FDSOI has shown an excellent noise behavior caused by its un-doped channel and the buried oxide (BOX). However, the un-doped channel has to be carefully optimized to deliver the needed performance especially in the higher power regime.

In this work, both technologies are investigated with regard to their small-signal behavior. Chapter II describes the structures and chapter III their process optimization. In Chapter IV the various biasing methods of the FDSOI are examined as non-process optimization alternatives. A second focus of this chapter is on the improvement of the transistors noise behavior, supported by the assumption that noise can be modulated by carrier distribution [7]. The buried channel on the Bulk side and the additional back gate on the FDSOI side are assumed to show comparable effects.

II. TRANSISTOR DESIGN

The schematic of the simulated FDSOI architecture is shown in Fig. 1. It consists of a <12 nm un-doped SOI substrate with a BOX ~20 nm. The gate oxide (GOX) is an industrial standard HKMG with a thickness between 40 and 70 Å.

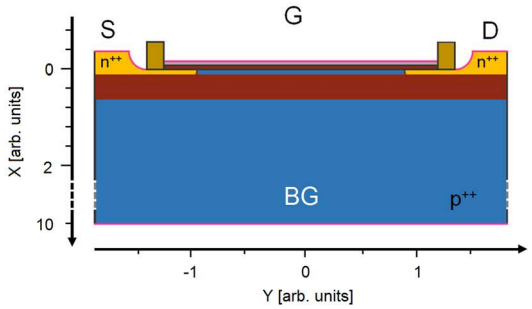

Fig. 1: Cross section of the 250 nm nMOS FDSOI device with HKMG, epitaxially grown S/D regions for lower contact resistance.

A second structure is simulated based on a BC Bulk transistor as a reference. Its schematic is shown in Fig. 2. The substrate includes a thin layer, which is slightly n-doped. The purpose is to shift the current flow towards the n-doped implant away from the Si/SiO_2 interface. Hence, the random telegraphic noise is decreasing and the overall low frequency noise performance can be improved [4]. This implant improves the noise behavior of the transistor, but degrades the transconductance compared to the original bulk structure, as any additional doping contributes to the decrease in carrier acceleration.

Sentaurus Process and Device have been used for TCAD simulations [5]. The quantum-drift-diffusion framework including density gradient model was applied and thin-layer-mobility model was added for SOI structures. The calibration was done with respect to 22 nm-baseline measurements.

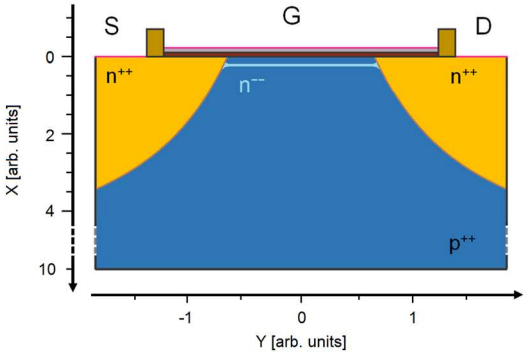

Fig. 2: Cross section of the 250 nm nMOS Bulk device with slightly n-doped buried channel implant for RTN performance improvement.

III. Process Optimization Results

The process of the FDSOI devices has been optimized to improve the small-signal parameter g_m. Several process variations are investigated and adjusted while adopting the best results. The variations of SOI film and GOX showed the highest improvements. The results are presented in Fig. 3.

The g_m increase driven by the thicker SOI film is limited since V_{th} and I_{off} increase. In applications where low power consumptions are required the SOI film cannot become too thick. Another improvement was achieved by reducing the GOX thickness. In addition, the DC targets were maintained. V_{th} and I_{off} decreases with an increase of g_m. The thinner oxide increases the gate capacity, which increases the drain current and thus g_m. Therefore, a thick Si film and a thin GOX are used for the optimized FDSOI structure. At low voltage the device achieves a transconductance higher than the BC Bulk while showing a slightly lower g_m at higher operating voltages.

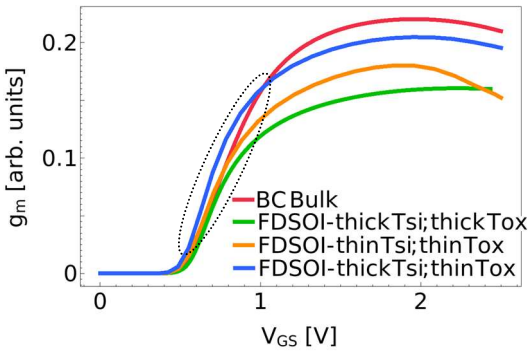

Fig. 4: g_m vs. V_{GS}: The FDSOI device shows a higher channel control at low voltage supply by combining the individual optimized layer thickness (V_{GS} = 0.6-1.0 V).

IV. Non-Process Related Optimizeations

Beside process optimization, FDSOI offers the back gate biasing mode (BGM) and biasing front and back gate equally in double gate mode (DGM).

Fig. 5 illustrates the g_m curves at different back gate biasing points. It clearly shows the shift of the threshold voltage V_{th} with change of the back gate voltage. As back gate voltage increases (forward back bias), the threshold voltage decreases.

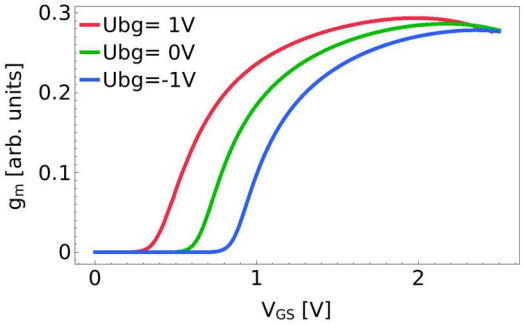

Fig. 5: g_m of the FDSOI transistor at different back gate voltages.

The electron density distribution in Fig. 6 explains the shift of the threshold voltage towards smaller values with positive back gate biasing. When the back gate is biased in forward direction it starts to invert the channel at the back interface. This explains the even carrier distribution within the channel at a low drain current. The highest g_m is achieved at this biasing point and the risk of trapping is minimized because of fewer carriers near the oxides. In reverse back bias, when the back gate is biased with a negative voltage, the carriers are pushed closer to the front gate, what increases trapping at the GOX.

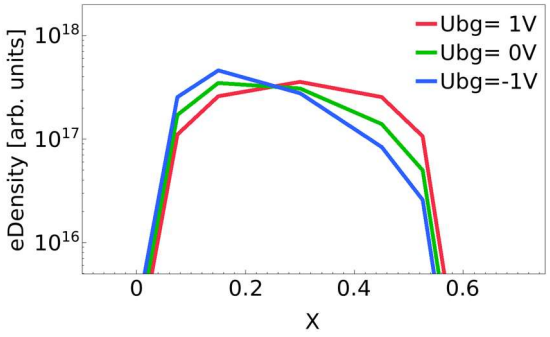

Fig. 6: Electron density distribution of the FDSOI transistor simulated at 5µA I_D with different BGM voltages.

An extended but similar principle can be seen in the synchronous biasing of front and back gate in DGM. Here the conventional front gate biasing (FGM) of the FDSOI is compared with DGM biasing in Fig. 7. A higher electron density distributed over the entire channel can be achieved in DGM. By connecting both gates in parallel, the effective gate area got increased and an additive behavior of the capacities can be assumed. The electron distribution forms almost a plateau. This is only distorted by a stronger influence of the front gate. In turn, this distribution contributes to higher channel control.

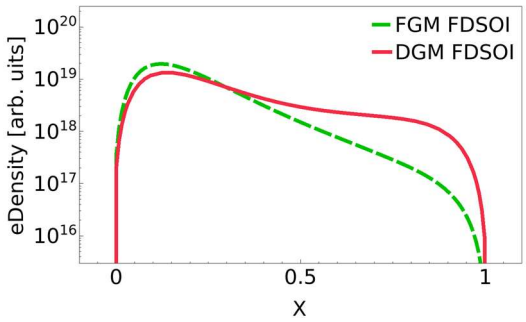

Fig. 7: Electron density distribution of the FDSOI transistor in FGM and DGM simulated at 5µA I_D. The lower electron density at the same current near the front gate of the DGM FDSOI indicates higher charge carrier mobility in comparison to the FGM FDSOI.

Beside better channel performance both biasing options of the FDSOI, BGM and DGM, contribute to better noise performance. Comparable to a BC Bulk transistor, forward back biasing shifts charge carriers away from the oxide-substrate-surface. Thus less trapping can be assumed. DGM shows a similar effect. This must be considered in relation to the trapping caused by the BOX. Therefore, it can be assumed that a ratio of front and back gate that is as equal as possible, contributes to the best noise behavior. BGM or DGM should be used depending on the application.

The intrinsic gain (g_m/I_D) is used for a better comparison of the different device architectures. Fig. 8 shows the optimized standard structure and the DGM biased FDSOI device as well as the BC Bulk transistor at the moderate inversion regime (MI). In this regime a certain balance between power consumption and speed is given [6]. The optimized FDSOI device shows the best g_m/I_D behavior in weak (WI) and moderate inversion, which are mainly used for analog applications. When synchronizing front and back gate, the intrinsic gain can be increased even further [7].

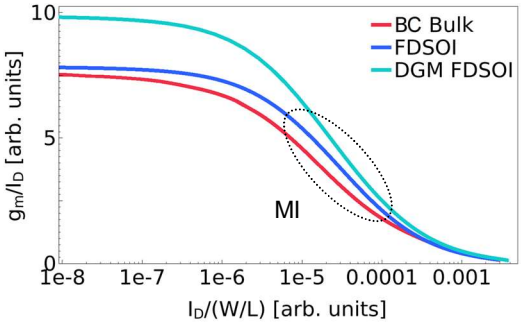

Fig. 8: g_m/I_D vs. $I_D/(W/L)$: In the moderate inversion regime and above the FDSOI device shows a drastically increase of the intrinsic gain g_m/I_D compared to the conventional BC Bulk device.

V. SUMMARY

This analysis shows the suitability of FDSOI devices for analog applications which require low power consumption while maintaining a high transconductance g_m as well as lowest Low Frequency Noise behavior. The FDSOI has an increased g_m/I_D in MI and WI compared to the conventional Bulk transistor having its architecture especially its capacitance ratio optimized. The ability to bias the back gate in DGM even further increases the intrinsic gain with small additional layout efforts and builds a strong opponent against the BC Bulk in terms of noise improvement.

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