Suppression of the Corner Effects in a 22 nm Hybrid Tri-Gate/Planar Process

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***Abstract*: A hybrid Tri-Gate/planar process was investigated by 3-D process and device simulations. Electrostatics of a Tri-Gate and a planar transistor sharing the same well, halo, and S/D have been compared. The suppression of the Tri-Gate corner effect was studied by corner implantation and additional corner rounding after Tri-Gate fin formation. Corner implantation is useful for retargeting Tri-Gate threshold voltage independent of shared planar implantation settings. Corner rounding allows a reduction of electric field overlap, suppressing corner leakage path and improve I_{ON}-I_{OFF} performance.**

I. Introduction

The scaling of CMOS technologies reaches the 22 nm node and even the most optimized planar MOSFETs show degraded electrostatic behavior at short channels [1]. For future scaling to the end of the ITRS roadmap, novel transistor structures are required to improve electrostatic integrity with gate lengths shorter than 20 nm [2-4]. Classical FinFETs with high aspect ratio are difficult to implement into existing planar process flows [5]. A Tri-Gate transistor with low-profile fins has the advantage of being more compatible with existing process flows and can be co-processed with planar MOSFETs [6]. Therefore Tri-Gates could be used as short-channel high-performance devices or in low-voltage circuitry, planar transistors are maintained for long channel applications such as analog and I/O. This Tri-Gate/planar hybrid concept allows design portability into a CMOS technology with 3-D transistors, which is very important for SoC time to market.

Ideally, a Tri-Gate process flow could even be run without any additional masking, by sharing implantations and metal gate work function metals with planar transistors. In this work 3-D simulations (Sentaurus D-2010.03) are used to study the electrical behavior of Tri-Gates built into a bulk planar process. Tri-Gates with shared wells, extensions, halos, insitu-doped epitaxial S/Ds, and dual band-edge metal gate work functions have been simulated versus geometrical parameters such as fin height and width [7]. Tri-Gates V_{th} and I_{OFF} are affected by overlapping Top- and Side-Gate electric fields at the Tri-Gate corner. This corner effect needs to be suppressed by additional corner implantation and/or corner rounding. Corner implantation uses the fin formation hardmask and allows a retarget of Tri-Gate threshold voltage independent of the halo implantation shared with the planar MOSFETs. Corner rounding erases electric field overlapping of Top- and Side-Gate and permits a homogenous transition between Top- and Side-Channel. The resulting Tri-Gate built into a planar process shows improved electrostatic behavior, excellent control of threshold voltage by corner implantation and allows scaling of L_{gate} with less drive current and V_{th} mismatch degradation compared to planar.

II. Device Structure

A planar CMOS process was first simulated in 3-D around 22 nm technology ground rules with an assumed nominal $L_{gate} = 26$ nm and $T_{ox,inv} = 1.0$ nm, in line with ITRS assumptions. Extension, halo, epitaxial S/D, and anneal conditions were tuned for good electrical integrity of planar MOSFETs, with $I_{OFF} = 40$ nA/µm and a subthreshold slope ca. 90 mV/dec. This study focuses on the NMOS results only, since similar trends apply to PMOS.

Additional steps were then added to the 3-D planar process simulation to create a Tri-Gate structure, as shown in fig. 1. After Tri-Gate formation, it is assumed that a planar FET and Tri-Gate would run the identical process.

- STI
- Well implantations
- Tri-Gate fin formation with corner implantation
- Corner rounding
- Dummy gate patterning
- S/D extension and halo implantations
- eSiGe module
- NMOS raised S/D module
- Activation anneal
- Replacement gate
- Silicidation and contacts

Fig. 1: *Process sequence of 22 nm hybrid Tri-Gate/planar process.*

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Fig. 2 illustrates a slice of NMOS Tri-Gate transistor after the process simulation with a corner radius of 5 nm and resulting dopant profile nearly identical to that of the planar transistor.

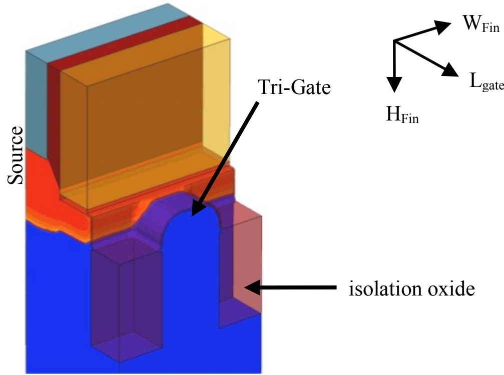

Fig. 2: *Slice of a simulated n-Tri-Gate transistor with 5 nm corner radius.*

III. Results and Discussion

A. Simulation of Tri-Gate corner effect

For the comparison between a planar and a Tri-Gate NMOS, and to analyze the Tri-Gate corner effect, we simulated both types of structures with a total width of 50 nm and nominal gate length of 26 nm. The Tri-Gate width and height was set to 20 nm. The planar transistor shows a decent subthreshold slope of 90 mV/dec and 97 mV/V DIBL. The Tri-Gate structure had a subthreshold slope of 72 mV/dec and much smaller DIBL of 49 mV/V. The significance of the enhanced electrostatic behavior of the Tri-Gate is illustrated in fig. 3. While the planar FET has strong $V_{th,sat}$ rolloff to sub-nominal, the Tri-Gate rolloff curve remains relatively flat.

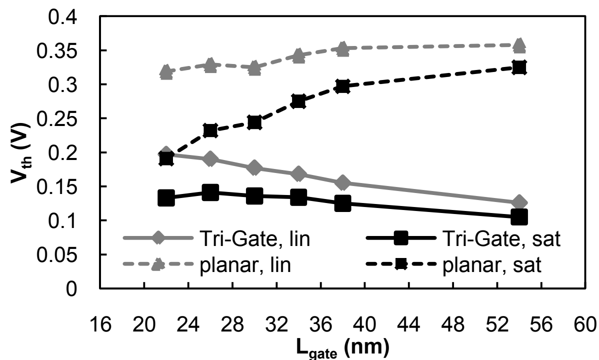

Fig. 3: *Simulated roll-off curve for a planar and Tri-Gate transistor (W_{Fin} = 25 nm, H_{Fin} = 20 nm)*

But the Tri-Gate threshold voltage at all simulated gate lengths is lower due to the improved subthreshold slope and the corner effect [8]. The corner effect is a result of increased segregation and out-diffusion of boron dopants and the overlapping electric fields of Top- and Side-Gate at the Tri-Gate corner. Both effects result in a higher electrostatic potential, lower conduction band energy and an increased carrier density at the corner (fig.4).

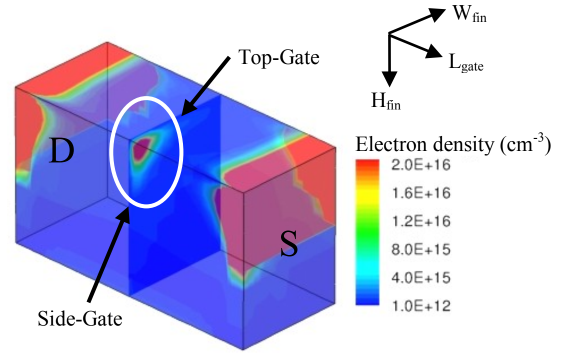

Fig. 4: *Simulated electron density for a n-Tri-Gate cutted at the half transistor width (V_{GS} = 0 V, V_{DS} = 0.8 V)*

B. Corner Implantation

One method to control the corner effect of Tri-Gate transistors, without changing planar implantation settings such as halo dose, is a special corner implantation. It can be realized prior to Tri-Gate fin formation. The lateral scattering of a non-tilted low-energy implantation can be used to dope the corner region of the Tri-Gate fin lying under the fin patterning hardmask.

The higher doping compensates the segregation and out-diffusion of boron dopants, and the increased electrical field. The electrostatic potential of the corner region can be matched to potential at the center of the Top- and Side-Channels, and thus the threshold voltage can be matched to the planar transistors at lower I_{OFF} (fig. 5).

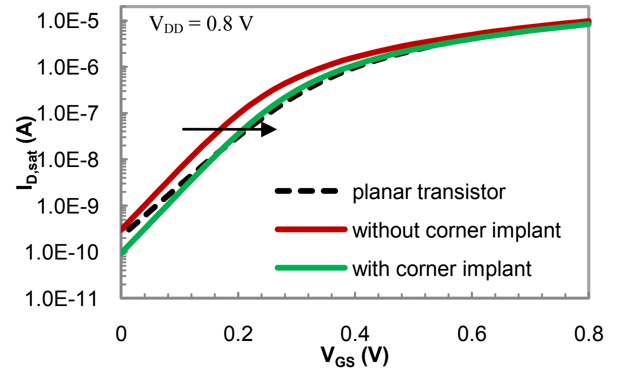

Fig. 5: *Drive current of a NMOS Tri-Gate with (5e13 cm^{-2}, BF2) and without a corner implantation. The planar transistor shows a reference behavior with the same effective gate width of 34 nm (L_{gate} = 26 nm).*

The corner effect has a strong dependence on the fin height and is increased for tall fins [7]. So the corner implantation must be adjusted by dose to target Tri-Gate threshold voltage to the planar reference. Fig. 6 shows the V_{th} behavior depending on fin height of Tri-Gates with different corner implantations.

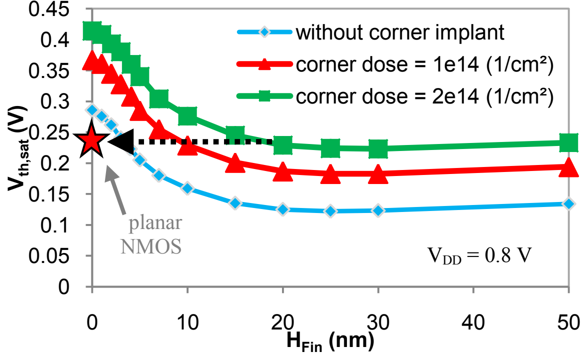

Fig. 6: *Threshold voltage of NMOS Tri-gates with different corner implantation doses in dependent of the fin height (L_{gate} = 26 nm).*

C. Corner Rounding

Another method to control the corner effect is to round the corners, allowing a homogenous transition between Top- and Side-Channel of the doping profile, and reduces the overlap of the and electrical fields. In addition, due to the corner rounding inherent in FEOL cleaning and etching, it is expected that the corner leakage effect will be effectively suppressed, as reported in [9-10].
In this work we simulated NMOS Tri-Gate transistors with a corner radius between 0 and 6 nm. Fig. 7 shows an increasing of threshold voltage until $V_{th,sat}$ = 200 mV resulting from reduced electric field overlap and suppressed leakage path. But the planar value of $V_{th,sat}$ = 230 mV could not be reached and the transistor loses electrostatic performance by an increased subthreshold slope. However, I_{OFF} can be matched to planar as shown in fig. 8.

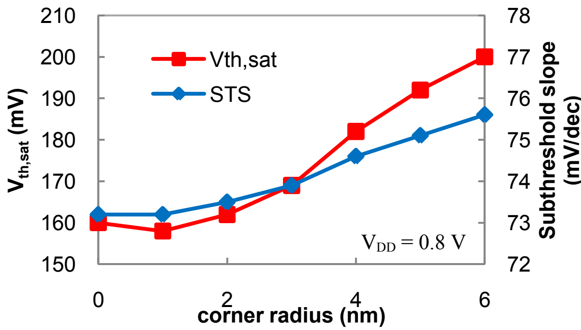

Fig. 7: *Behavior of Tri-Gate threshold voltage and subthreshold slope depending of corner radius. (H_{Fin} = 10nm, W_{Fin} = 20 nm, L_{gate} = 26 nm).*

The leakage path of corners is not placed at the surface of Top- and Side-Gate due to quantization effects and there for leakage and the currents are not changed until a corner radius of 2 nm (fig. 8). After that the corner leakage can be cut off shown by the percent change of total leakage between 2 and 5 nm corner radius. The leakage path is mostly eliminated with a corner radius of 5 nm or larger and the Tri-Gate transistor starts losing drive current.

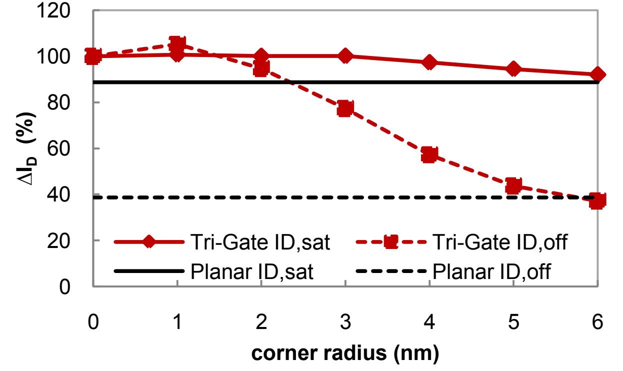

Fig. 8: *Percent change of drive current and leakage current depending of corner radius. (H_{Fin} = 10nm, W_{Fin} = 20 nm, L_{gate} = 26 nm).*

The best result was simulated for a NMOS Tri-Gate with 4 nm corner radius which has an improved I_{ON}-I_{OFF} performance demonstrated by the universal curve in comparison with a planar transistor and a Tri-Gate without corner rounding (fig. 9). Note that the gate length ranged from 34 to 22 nm and the transistor performance of rounded Tri-Gates allows a further scaling for sub 22 nm technologies.

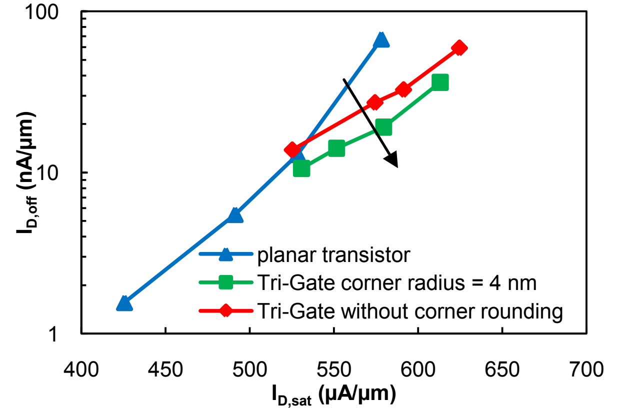

Fig. 9: *I_{ON}-I_{OFF} performance of NMOS Tri-Gate transistors with 4 nm corner radius and without corner rounding. (H_{Fin} = 10nm, W_{Fin} = 20 nm, L_{gate} = 22-34 nm).*

IV. Conclusion

A Tri-Gate approach of 22 nm ITRS technology assumptions with a planar process starting point was investigated in relation to additional corner implantation and different corner radii. Such an approach is the basis for a low-cost Tri-Gate/planar hybrid technology, where Tri-Gates and planar would share the same implantation masking, same S/D processes, and same dual band-edge metal gate work functions. A comparison between 3-D simulations of Tri-Gate and the planar transistors shows significantly better electrostatics and I_{ON}-I_{OFF} performance of the Tri-Gate NMOS with matched threshold voltage.
The threshold voltage offset of non-rounded Tri-Gate

transistors can be retarget by a simple low-energy corner implantation. The implantation uses the existing fin formation hardmask and offers a self-aligned doping correction of the increased segregation and out-diffusion of boron dopants at the corner regions.

The corner rounding inherent in FEOL cleaning at etching has been investigated by 3-D simulations of Tri-Gate transistors with different corner radii. The Tri-Gate with a rounded corner shows a significantly better I_{ON}-I_{OFF} performance due to homogenous doping profile transition between Top- and Side-Channel, reduced overlapping of electrical fields and cutoff of leakage paths. For a corner radius over 5 nm the corner leakage path is mostly eliminated.

The performance benefit of Tri-Gates and the cost benefits of sharing implantations between Tri-Gates and longer channel planar FETs are clear. However, this approach, and in particular the corner effect, is very sensitive to the height of the Tri-Gate which must be very well controlled in the process.

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