

NUMERICAL SIMULATION OF NANOSCALE DOUBLE-GATE MOSFETS

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ABSTRACT

The further improvement of nanoscale electron devices requires support by numerical simulations within the design process. After a briefly description of our 2D/3D-device simulator SIMBA, the results of the simulation of DG-MOSFETs are represented. Starting from a basic structure with a gate length of 30 nm, a calibration of model parameters was done based on measured values from literature. Afterwards a variation of gate length, channel thickness and doping, gate oxide parameters and source/drain doping was carried out in connection with the numerical calculation of device characteristics. Thereafter an optimization of a DG-MOSFET with a gate length of 15 nm was done. The optimized structure shows suppressed short channel behavior and short switching times of about 0.15 ps.

Keywords

Device simulation, semiconductor devices, double-gate MOSFET

NOTATION

p, n	hole and electron density
φ	electrostatic potential
N_A, N_D	ionized donor and acceptor density
ϵ_s	permittivity of semiconductor
q	elementary charge
$\mathbf{J}_p, \mathbf{J}_n$	current densities
R, G	recombination and generation rate
μ_p, μ_n	carrier mobilities
λ_p, λ_n	quantum correction potentials
Θ_p, Θ_n	band parameters
D_p, D_n	diffusion coefficients
T_p, T_n	carrier temperatures
k_B	Boltzmann constant
$\mathbf{S}_p, \mathbf{S}_n$	energy flux densities
\mathbf{E}	electric field strength
T_L	lattice temperature
τ_{wp}, τ_{wn}	energy relaxation times
m_p, m_n	carrier effective masses
\hbar	reduced Plancks constant
γ_p, γ_n	quantum correction coefficient
κ_p, κ_n	thermal conductivities

INTRODUCTION

Double-Gate (DG) MOSFETs are considered to be one promising candidate for nanoscale CMOS. The International Technology Roadmap for Semiconductors (2005 Edition) predicts printed gate lengths up to 15 nm for the next 10 years. For these gate lengths conventional MOSFETs are limited due to different short channel effects. On the other hand structures with two gates and extremely thin body demonstrate a better control of the gate region and consequently a suppression of short channel effects.

Numerical device simulation is an important procedure for the design and optimization of novel semiconductor devices. Advantages are the calculation of the electrical behavior before the fabrication process, the calculation and visualization of inner-electronic values which are not measurable, the diagnosis/fault-detection in the technological process and consequently the cost efficiency.

SIMULATION MODELS

The quantum hydrodynamic (QHD) models, which are based on a quantum fluid dynamic model, offers expanding possibilities for the understanding as well as the design of quantum sized semiconductor devices. The advantage of this model is its macroscopic character, which enables to obtain description without knowledge of

quantum mechanical details like initial wave function [1], [2], [3]. The classical hydrodynamic (HD) model for the semiconductor device simulation can be extended by expressions in the transport and in the energy balance equations. They describe an internal quantum potential in the transport equation as well as a quantum heat flux in the energy balance equation. These additional terms in the classical hydrodynamic model allow to describe continuous electron and hole distribution in a semiconductor device, accumulations of carriers in potential wells and resonant tunneling of carriers, respectively. The standard model for universal device simulations is the drift-diffusion (DD) model, which can be derived from the above mentioned model [4].

Basic equations of the QHD model are the Poisson equation

$$\nabla(\epsilon_s \nabla(\varphi)) = -q(p - n + N_D - N_A) \quad (1)$$

continuity equations (index p: holes, index n: electrons)

$$\nabla \cdot \mathbf{J}_p = -q \left(R - G + \frac{\partial p}{\partial t} \right) \quad (2)$$

$$\nabla \cdot \mathbf{J}_n = q \left(R - G + \frac{\partial n}{\partial t} \right) \quad (3)$$

transport equations

$$\mathbf{J}_p = -qp\mu_p \nabla(\varphi - \lambda_p - \Theta_p) - D_p q \nabla(p) - k_B p \mu_p \nabla(T_p) \quad (4)$$

$$\mathbf{J}_n = -qn\mu_n \nabla(\varphi + \lambda_n + \Theta_n) + D_n q \nabla(n) + k_B n \mu_n \nabla(T_n) \quad (5)$$

energy balance equations

$$\nabla \cdot \mathbf{S}_p = \mathbf{J}_p \cdot \mathbf{E} - \frac{3}{2} k_B p \frac{(T_p - T_L)}{\tau_{wp}} - \frac{3}{2} k_B \frac{\partial}{\partial t} (p T_p) - \frac{3}{2} k_B T_p (R - G) - \frac{1}{2} q \lambda_p \left(\frac{p}{\tau_{wp}} - (G - R) \right) - \frac{1}{2} q \frac{\partial}{\partial t} (p \lambda_p) \quad (6)$$

$$\nabla \cdot \mathbf{S}_n = \mathbf{J}_n \cdot \mathbf{E} - \frac{3}{2} k_B n \frac{(T_n - T_L)}{\tau_{wn}} - \frac{3}{2} k_B \frac{\partial}{\partial t} (n T_n) - \frac{3}{2} k_B T_n (R - G) + \frac{1}{2} q \lambda_n \left(\frac{n}{\tau_{wn}} - (G - R) \right) + \frac{1}{2} q \frac{\partial}{\partial t} (n \lambda_n) \quad (7)$$

energy flux density equations

$$\mathbf{S}_p = -\kappa_p \nabla(T_p) + \frac{5}{2} \frac{k_B}{q} T_p \mathbf{J}_p + \frac{3}{2} \lambda_p \mathbf{J}_p \quad (8)$$

$$\mathbf{S}_n = -\kappa_n \nabla(T_n) - \frac{5}{2} \frac{k_B}{q} T_n \mathbf{J}_n + \frac{3}{2} \lambda_n \mathbf{J}_n \quad (9)$$

and equations for the quantum correction potential

$$\lambda_p = -\frac{\gamma_p \hbar^2}{6 m_p q} \frac{\nabla^2 \sqrt{p}}{\sqrt{p}} \quad (10)$$

$$\lambda_n = \frac{\gamma_n \hbar^2}{6 m_n q} \frac{\nabla^2 \sqrt{n}}{\sqrt{n}} \quad (11)$$

Further approaches are necessary for carrier mobilities, generation and recombination rates, diffusion coefficients and energy relaxation times, which are almost material dependently. Equations (1) to (11) are solved self-consistently for the variables (φ , p , n , T_p , T_n , λ_p , λ_n). If equations (10) and (11) are neglected, that means for $\lambda_p = \lambda_n = 0$, QHD model can be reduced to the conventional hydrodynamic (HD) model. If carrier temperatures are set to lattice temperature and equations (6) to (9) are neglected, the quantum drift diffusion (QDD) model and additionally for $\lambda_p = \lambda_n = 0$ the conventional drift diffusion (DD) model can be obtained. Solution of the equations are achieved by a successive algorithm (so called Gummel algorithm). For the solution of the partial differential equations a box method is used. The resulting non-linear equation systems are solved by the

NEWTON-method and corresponding linear equation systems by preconditioned gradient methods. All models are implemented full three-dimensional in the program system SIMBA [5] [6].

BASIC STRUCTURE SIMULATION AND VERIFICATION

Starting point of the simulations is a basic structure, represented in Figure 1, as functional relevant detail of the real device. The different parameters are assumed as following: gate length $L_G = 30$ nm, source/drain lengths $L_S = L_D = 100$ nm, gate-to-source and gate-to-drain distances $L_{GS} = L_{GD} = 100$ nm, silicon film thickness $T_{Si} = 20$ nm, gate oxide thickness $T_{ox} = 2$ nm, channel doping $N_A = 1 \cdot 10^{16} \text{ cm}^{-3}$, source/drain doping $N_D = 3 \cdot 10^{20} \text{ cm}^{-3}$.

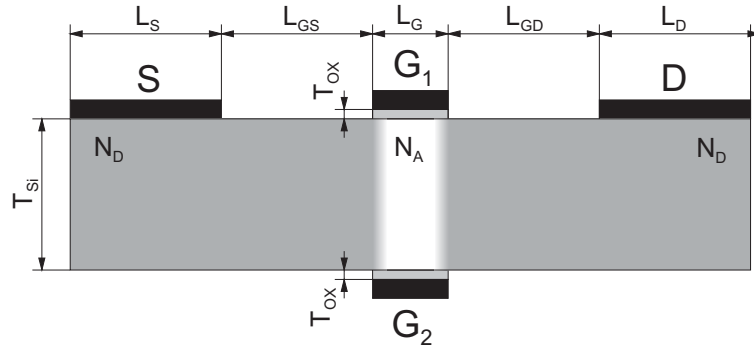


Fig. 1: Basic structure of the DG-MOSFET

The simulated output characteristics drain current I_D versus drain-to-source voltage V_{DS} are plotted in Figure 2 for different gate-to-source voltages V_{GS} . Verification of the simulation results and calibration of the model parameters were done by comparison with experimental values from [7]. A structure similar to Figure 1 with $L_G = 45$ nm, $T_{ox} = 2.5$ nm, $N_D = 2 \cdot 10^{20} \text{ cm}^{-3}$ was simulated and compared with the measured values. The results represented in Figure 3 show a good agreement. A further successful verification was done by results from [8].

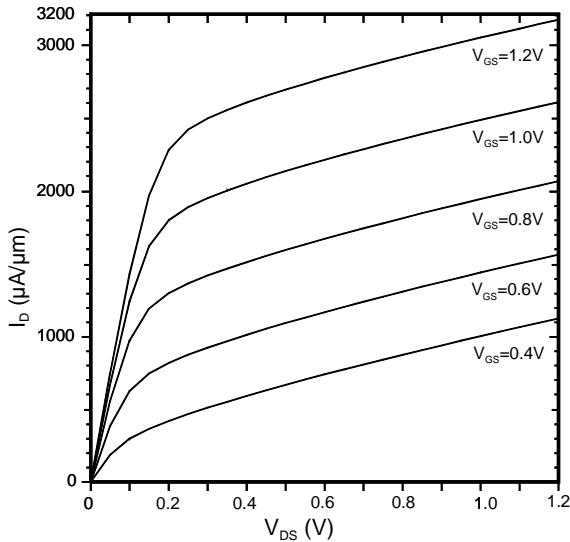


Fig. 2: Output characteristics of the basic structure

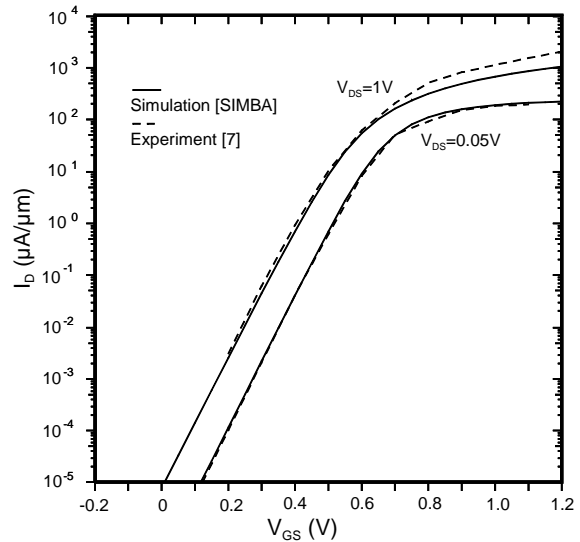


Fig. 3: Transfer characteristics - Simulation and experiment

PARAMETER VARIATION AND OPTIMIZATION

To study the influence of the structure parameters on the electrical device characteristics different parameters are modified. In Figure 4 and 5 the output and the transfer characteristics at different gate lengths are depicted. At shorter gate lengths a threshold voltage roll off can be observed as a typical short channel effect in particular pinch-off behavior disappears for $L_G < 30$ nm. At the same time drain saturation current increases strongly.

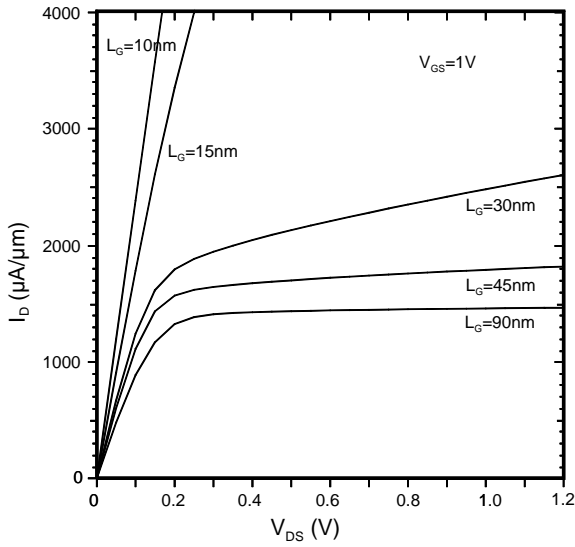


Fig. 4: Output characteristics at different gate lengths

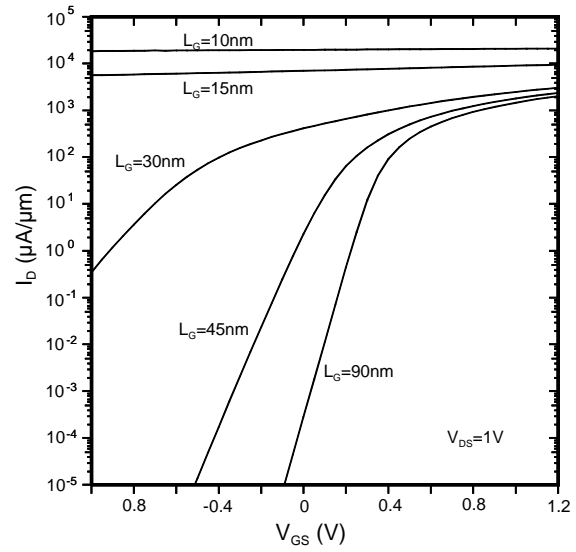


Fig. 5: Transfer characteristics at different gate lengths

Variation results of the silicon film thickness are represented in Figure 6. Thicker channels lead to larger drain currents but also to a displacement of the threshold voltage toward smaller values. Therefore the film thickness should be not larger than 20 nm. Thinner gate oxides result in increasing drain currents (Figure 7) and transconductances and in a better pinch-off behavior. According to that the smallest possible oxide thickness should be applied.

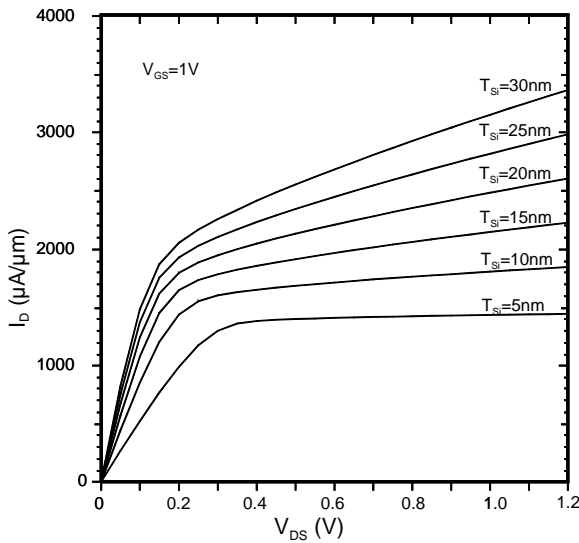


Fig. 6: Output characteristics at different channel thickness

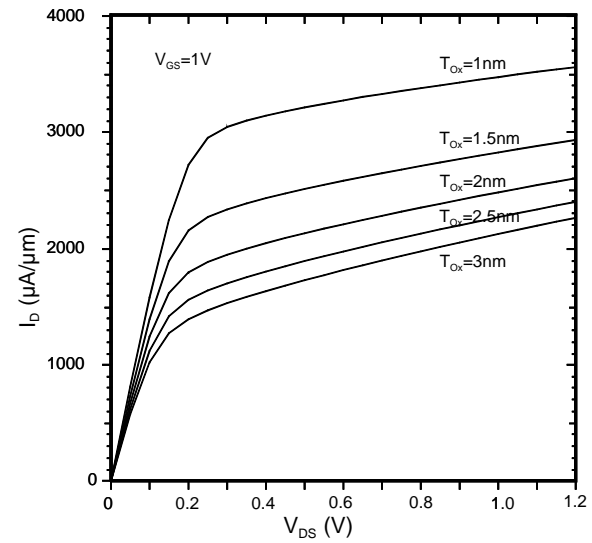


Fig. 7: Output characteristics at different gate oxide thickness

Variation of the channel doping causes a decrease of the drain current for doping densities greater than 10^{17} cm^{-3} (Figure 8). Furthermore the threshold voltage is strongly influenced by doping changes. For optimization of the structures, channel doping can be used to adjust the required threshold voltage. The source/drain doping should be high enough to reduce series resistances whereas the dopant diffusion into the channel has to minimize to prevent short channel effects. In this case rapid thermal annealing processes are an essential requirement. Figure 9 shows the corresponding output characteristics.

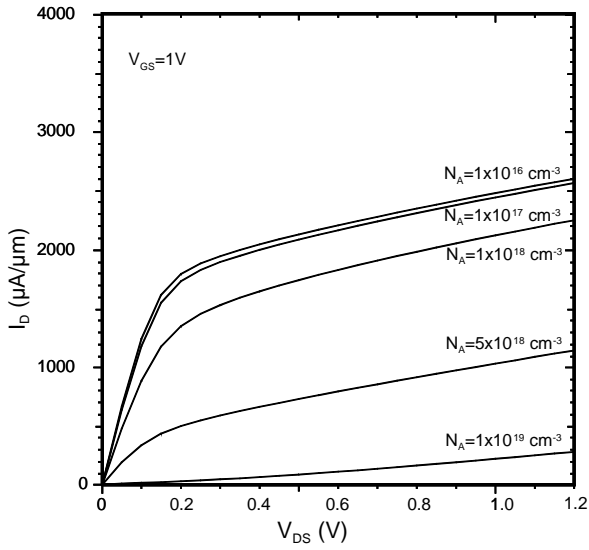


Fig. 8: Output characteristics at different channel doping

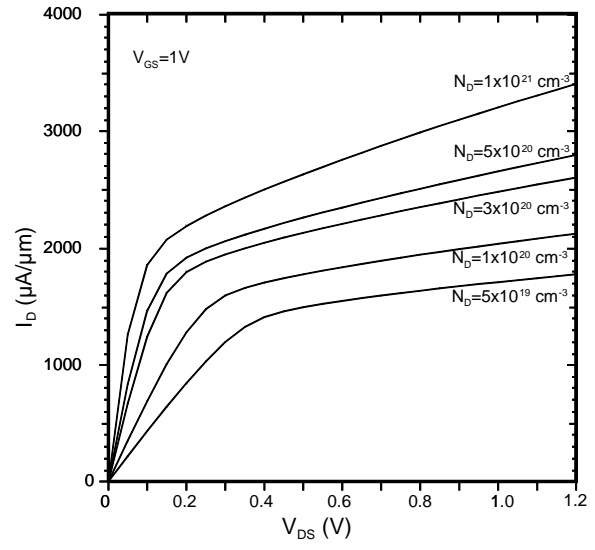


Fig. 9: Output characteristics at different source/drain doping

The knowledge from different variations was used for the design of an optimized structure. A minimal technologically practicable gate length of $L_G = 15$ nm and a gate oxide thickness of $T_{ox} = 1.5$ nm are specified. Further objectives are threshold voltage of $V_{Th} = 0.1$ V, large drain saturation current and improved dynamical behavior. After several iterations the further parameters are determined as follows: $T_{Si} = 3$ nm, $N_A = 2.8 \cdot 10^{19} \text{ cm}^{-3}$, $N_D = 7 \cdot 10^{20} \text{ cm}^{-3}$. The resulting output characteristics are represented in Figure 10. Figure 11 shows the comparison between transfer characteristic of the optimized and basic structure. An enlarged drain current as well as an improved transconductance can be observed.

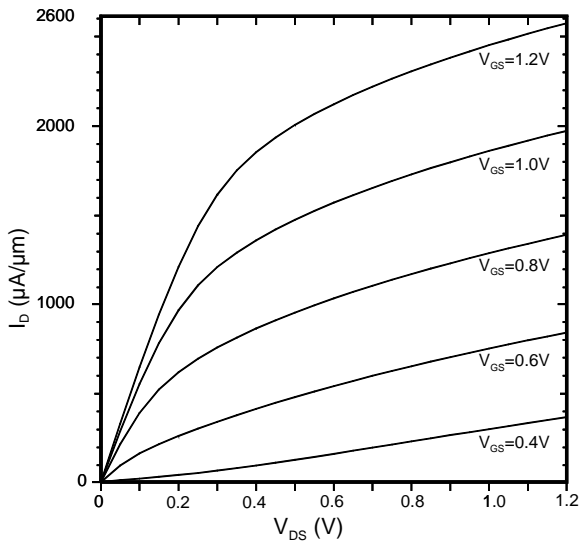


Fig. 10: Output characteristics of the optimized structure

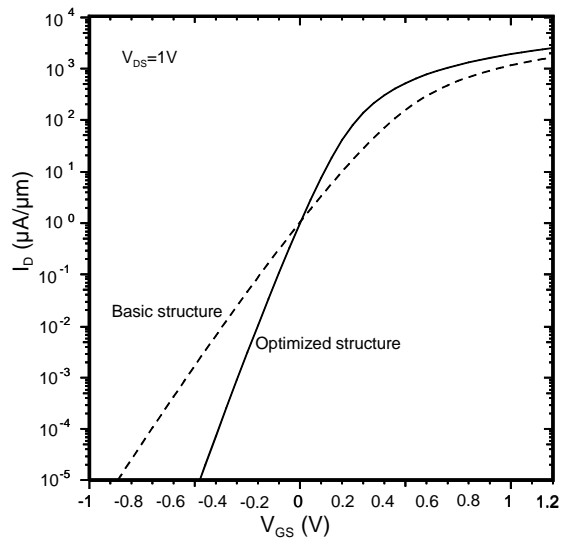


Fig. 11: Transfer characteristics of the basic and the optimized structure

For the determination of the dynamical behavior the gate-to-source voltage was switched from 0 V to 1 V to find the turn-on time (t_{ON}) and from 1 V to 0 V to find the turn-off time (t_{OFF}). Figure 12 shows the time response of the drain current. Therefrom the switching times result to $t_{ON} = t_{OFF} = 0.15$ ps. Compared with the basic structure the switching times are reduced by the factor 0.6 due to the structure reduction primarily.

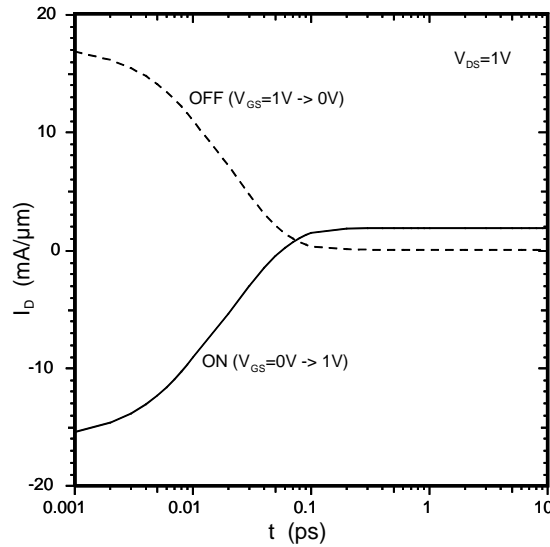


Fig. 12: Switching behavior of the optimized structure

CONCLUSION

The scaling down of planar bulk MOSFETs according to the International Technology Roadmap for Semiconductors requires new structures such as multiple-gate MOSFETs. One of the promising possibilities are double-gate transistors. The implementation will be challenging with numerous new and difficult issues. In this case numerical device simulation is essential. Variations of different structure parameters have been carried out to calculate the influence on device characteristics. Based on these results an optimized structure with a gate length of 15 nm was created. The optimized structure shows suppressed short channel effects and switching times of about 0.15 ps.

REFERENCES

- [1] Gardner, C.L.: *The quantum hydrodynamic model for semiconductor devices*. SIAM J. Appl. Math., **54** (2), 1994, p. 409-427.
- [2] Chen, Z.: *A finite element method for the quantum hydrodynamic model for semiconductor devices*. Comput. Math. Appl., **31**, 1996, p. 17-26.
- [3] Wettstein, A. - Schenk, A. - Fichtner, W.: *Quantum device simulation with the density-gradient model on unstructured grids*. IEEE Trans. Electron Devices, **48** (2), 2001, p. 279-284.
- [4] Selberherr, S.: *Analysis and Simulation of Semiconductor Devices*. Berlin, Germany, Springer-Verlag 1984.
- [5] Klix, W. - Stenzel, R.: *SIMBA-User Manual*. <http://www.htw-dresden.de/~klix/simba/welcome.html>.
- [6] Höntschel, J. - Stenzel, R. - Klix, W.: *Simulation of quantum transport in monolithic ICs based on $In_{0.53}Ga_{0.47}As-In_{0.52}Al_{0.48}As$ RTDs and HEMTs with a quantum hydrodynamic transport model*. IEEE Trans. on Electron Devices, **51** (5), 2004, p. 684-692.
- [7] Lee, J.H., et al: *Super self-aligned double-Gate (SSDG) MOSFETs utilizing oxidation rate difference and selective epitaxy*. IEDM, Tech. Digest, 1999, p. 3.5.1-3.5.4
- [8] Vinet, M., et al: *Bonded planar double-metal-gate NMOS transistor down to 10 nm*. IEEE Electron Device Letters, **26** (2005), p. 317-319