A Physical-Based PSPICE Compact Model for Poly(3-hexylthiophene) Organic Field-Effect Transistors

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***Abstract*—A PSPICE model for organic thin-film transistors (OFETs) employing poly(3-hexylthiophene-2,5-diyl) (P3HT) is derived. This model is based on the standard MOSFET Berkeley Short-channel IGFET Model equations, where the voltage dependences of the charge carrier mobility and the bulk conductivity are modeled by additional voltage-controlled current sources. The model requires only five additional parameters, which can be extracted from the output characteristics of the device. The model equations have been verified by device simulations, and the simulation results have been compared with measurements of P3HT OFETs.**

***Index Terms*—Compact model, organic thin-film transistors (OFETs), poly(3-hexylthiophene) (P3HT), SPICE.**

I. Introduction

THE RESEARCH in organic electronics has lead to the development of integrated circuits based on organic materials, for instance, active-matrix organic light-emitting diodes or radio-frequency identification tags. An important tool for the development of such complex organic integrated circuits is simulation programs such as SPICE that allow for accurate prediction of the electrical behavior even while changing working conditions or varying internal parameters. Since the quality of the simulation results depends on the models used, an accurate description of the physical effects is required. For example, models are defined according to variable range hopping of polarons [1], multiple trapping and thermal release [2], bandlike transport [3], or percolation theory [4]. However, the complex nature of these models representing intrinsic phenomena makes it difficult to implement these models in circuit simulators. On the other hand, simple device models such as the SPICE model in [5] and the compact static equivalent organic thin-film transistor (OFET) circuit diagram in [6] are only valid for a limited range of operation as some of the fixed model parameters still vary with a changing gate bias. One important contribution to the modeling of OFETs for circuit design, yielding a circuit model, was presented by Fadlallah *et al.* [7]. Here, the charge carrier mobility was modeled by a dependence on the carrier concentration. From this dependence, I–V equations were derived and implemented into a VERILOG model. As mentioned in that paper, it is important to find the right compromise between the physical approach and model convergence in circuit design. While laying emphasis on the convergence criterium, we follow a top–down approach, adding simple modifications to a standard Berkeley Short-channel IGFET Model (BSIM).

Therefore, we will show that a simple PSPICE model for OFETs using poly(3-hexylthiophene-2,5-diyl) (P3HT) can be derived from experimental data. We first describe the preparation and characterization of these devices. After that, we discuss the simulation results obtained by the drift-diffusion device simulator SIMBA, which indicate that the gate voltage dependence of the charge carrier mobility and the bulk conductivity have a significant influence on the transistor behavior. Subsequently, these simulation results are then utilized to deduce modifications of the MOSFET equations. Finally, these equations are implemented in a PSPICE subcircuit, which allow for a convincing agreement between the model and experimental results.

II. Device Fabrication and Characterization

The transistor electrodes are set up on silicon wafers consisting of highly n-doped silicon acting as the gate electrode and thermally grown silicon oxide with a thickness of 300 nm as the gate dielectric ($C'_{\mathrm{OX}} = 1.151 \cdot 10^{-8}\ \mathrm{F} \cdot \mathrm{cm}^{-2}$). The source and drain are deposited by thermal evaporation of chromium (10 nm) for adhesion purposes and subsequently of 50-nm gold through a shadow mask ($l = 26\ \mu\mathrm{m}, w = 1500\ \mu\mathrm{m}$). P3HT is spin-coated from a chloroform solution, yielding a film with a thickness of approximately 50 nm. Electrical characterization is performed using an Agilent 4156C parameter analyzer for current–voltage measurements in accordance with [7]. A closer examination of the output characteristics of the devices shows deviations from the ideal Si-MOSFET behavior, which are typical for OFETs. The two most important deviations are the nonquadratic increase of I_D with V_{GS} [8] and the increase of drain current I_D with increase of drain–source voltage V_{DS}

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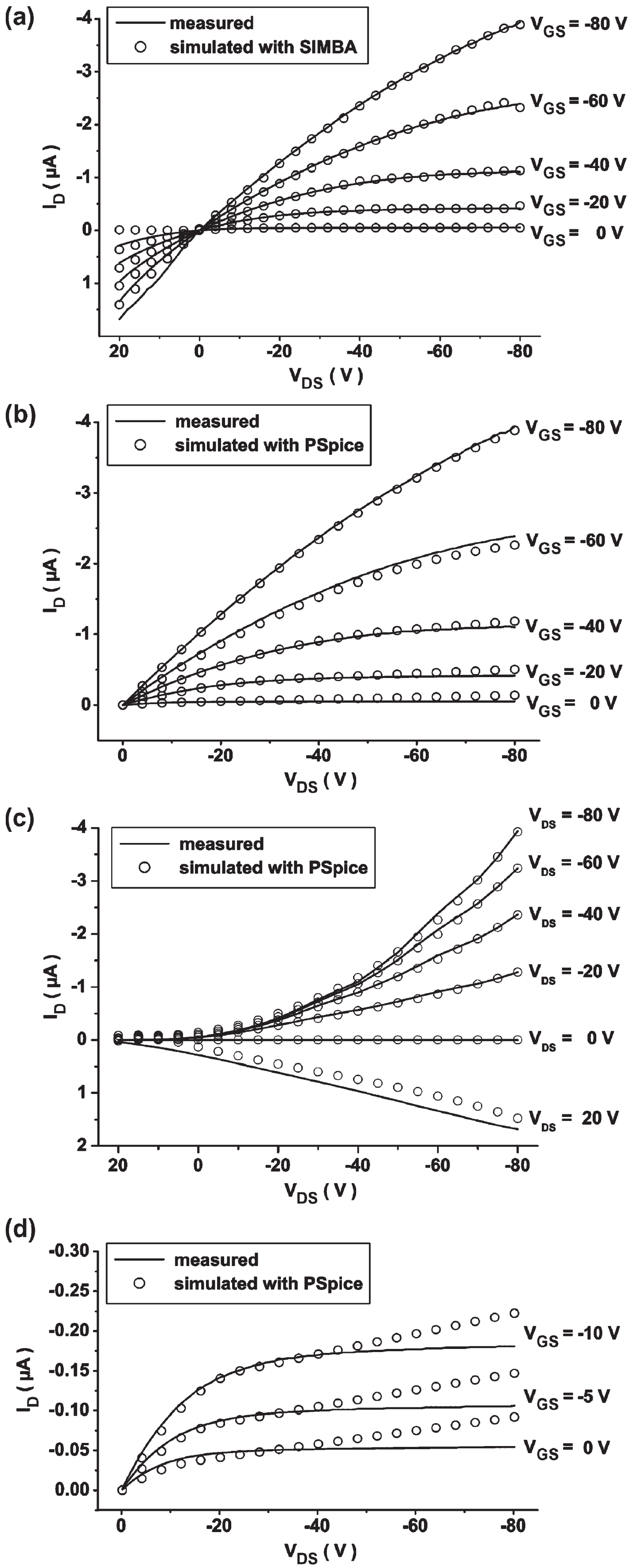

Fig. 1. Measured and simulated current–voltage characteristics. (a) Numerical simulation with the device simulator SIMBA. (b) PSPICE simulation of the output and (c) transfer characteristics. (d) PSPICE simulation of the output characteristics for $|V_{\mathrm{GS}}| \leq 10$ V.

in the saturation regime. It has to be noted that the latter effect cannot be attributed to the short-channel effect as in Si-MOSFETs but is caused by an increase of the number of charge carriers in the bulk material and thus an increase of the bulk conductivity.

III. DERIVATION OF MODEL EQUATIONS

In order to get analytical equations describing the aforementioned effects, we use the device simulator SIMBA to investigate the electrical behavior of the OFETs. The device simulator SIMBA solves a set of equations consisting of Poisson, continuity, and transport equations for electrons and holes, based on the so-called drift-diffusion model [9]. These sets of equations can either statically or dynamically be solved for the 3-D, as well as for the 2-D, case with the help of a box method. Since SIMBA is not designed for the simulation of organic semiconductors, the simulator has to be modified in accordance with [10]. This means, in particular, that both the charge carrier mobility and the carrier density depend on the gate bias. Simulating the measured characteristics with these adjustments yields the output characteristics given in Fig. 1(a), which are in good agreement to the measured curves. In the next step, the aforementioned modifications of the device simulator have to be transferred in mathematical equations, which can be implemented in the circuit simulator PSPICE. As emphasis is laid on practical relevance and extensive physical models are neglected, we focus on analytical equations that allow for a simple parameter extraction, in accordance with [11], and a transparent implementation in PSPICE. To implement the first modification—the gate-voltage-dependent carrier density—in PSPICE, we use a voltage-dependent bulk conductance G_{par} parallel to the source and drain contacts [5], [6]. This conductivity depends on V_{GS}, as shown in Fig. 2(a). The measured values can be approximated by the simple equation

$$G_{\mathrm{par}}(V_{\mathrm{GS}}) = G_0 \exp(V_{\mathrm{GS}}/V_{G0}) \tag{1}$$

where G_0 and V_{G0} are the model parameters specific for the given transistor.

For the purpose of modeling the nonquadratic increase of the drain current and, hence, the influence of the gate-dependent charge carrier mobility, the contribution of the parallel conductance is subtracted from the measured curves. Subsequently, from the corrected curves, the mobilities are calculated by a fit with the MOSFET equations, with mobility μ as fitting variable for every V_{GS}. The extracted values $\mu(V_{\mathrm{GS}})$ are given in Fig. 2(b) and can analytically be approximated by

$$\mu(V_{\mathrm{GS}}) = \mu_0 - \mu_1 \exp(V_{\mathrm{GS}}/V_{\mu 0}). \tag{2}$$

Here, μ_0, μ_1, and $V_{\mu 0}$ are, again, the model parameters. The decrease of the mobility, which is neglected by the approximation in (2), can be explained as a virtual decrease, which is evocated by a parasitic series resistance [12]. It must be noted that this behavior is not universal for all kinds of organic semiconductors though and, in particular, has not been observed for "high-mobility" OFETs.

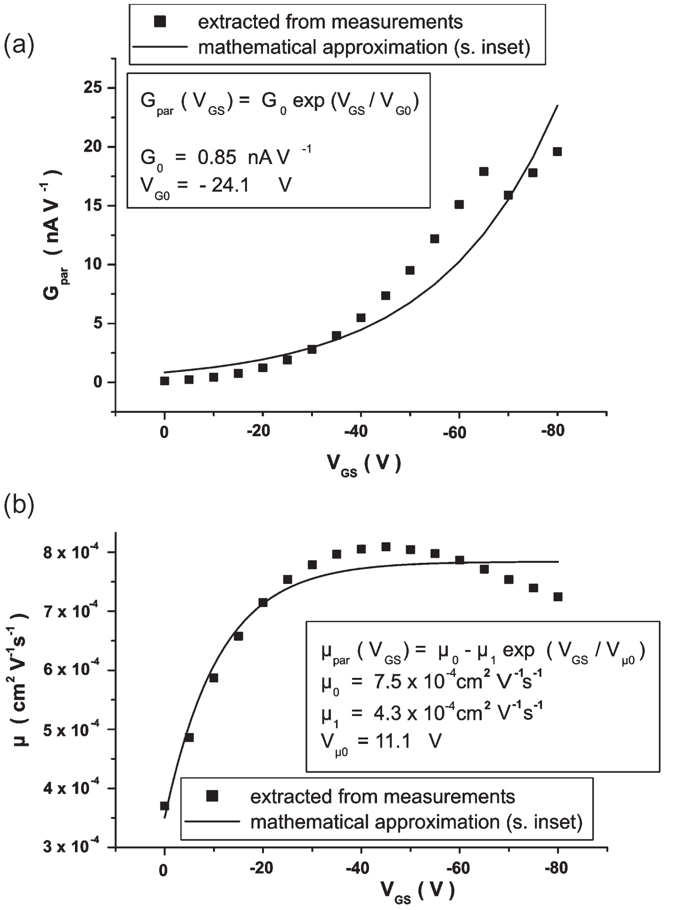

Fig. 2. Extracted values and mathematical approximation for the (a) parallel conductance G_{par} and (b) charge carrier mobility μ from measured output characteristics ($l = 26\ \mu$m, $w = 1500\ \mu$m, $C'_{\mathrm{OX}} = 1.151 \cdot 10^{-8}$ F $\cdot$ cm^{-2}).

The combination of (1) and (2) with the MOSFET equations yields an analytical description of the electrical behavior of OFETs with P3HT for the linear

$$\begin{aligned} I_D = & -\frac{W}{L} C'_{\mathrm{OX}}\, \mu(V_{\mathrm{GS}}) \\ & \times \left[(V_{\mathrm{GS}} - V_{\mathrm{th}})V_{\mathrm{DS}} - \frac{V_{\mathrm{DS}}^2}{2} \right] - G_{\mathrm{par}}(V_{\mathrm{GS}})V_{\mathrm{DS}} \end{aligned} \tag{3}$$

and the saturation regime

$$I_D = -\frac{W}{2L} C'_{\mathrm{OX}}\, \mu(V_{\mathrm{GS}})[V_{\mathrm{GS}} - V_{\mathrm{th}}]^2 - G_{\mathrm{par}}(V_{\mathrm{GS}})V_{\mathrm{DS}} \tag{4}$$

where W and L denote the width and length of the channel, respectively, and C'_{OX} is the insulator capacity per area. All other transistor parameters are independent of V_{GS}.

IV. PSPICE MODEL

In order to implement the model equations (1)–(4) in a PSPICE compact model, we use voltage-controlled current sources (VCCSs) describing the additional currents caused by the conductance modulation and mobility modulation [Fig. 3(a)].

In the case of the parallel conductance, G_{par} is modeled by a voltage-dependent resistor, which is realized by a multiplier

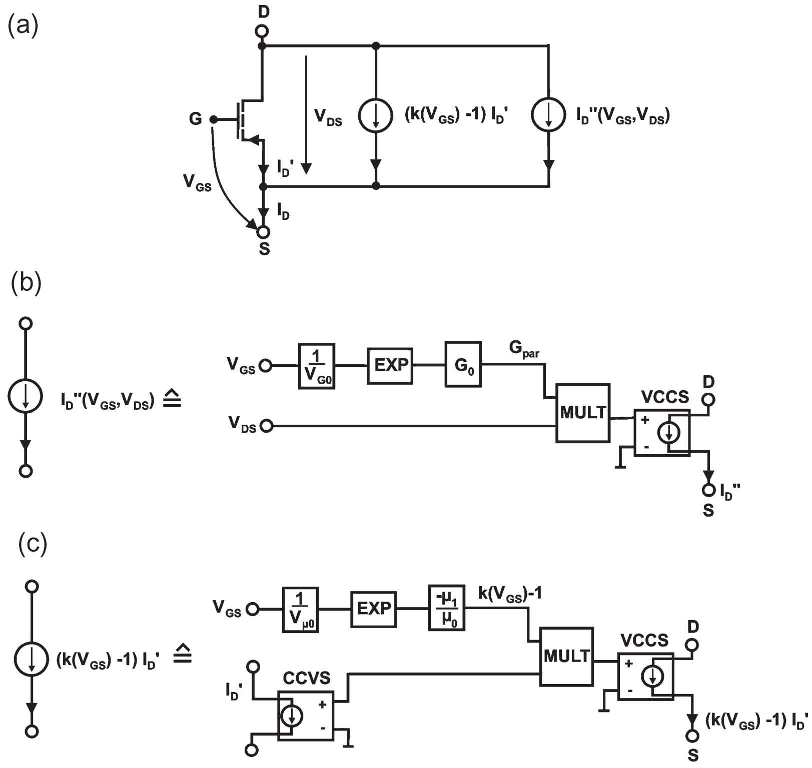

Fig. 3. (a) Equivalent circuit diagram of the organic FET and PSPICE building blocks of the equivalent current sources for the (b) gate-bias-dependent parallel conductance and (c) charge carrier mobility.

TABLE I
PSPICE NETLIST OF THE PRESENTED OFET MODEL

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.SUBCKT OFET D G S PARAMS: G0=0.85E-9 VG0=-24.1 Vu0=11.1 u1_by_u0=0.57

VD  D D2 DC 0

G1  D S VALUE { I(VD)*(-u1_by_u0)*exp(V(G,S)/Vu0)   }

G2  D S VALUE { V(D,S)*G0*EXP(V(G,S)/VG0)   }

M1  D2 G S S MP  L=26u  W=1500u

.model MP PMOS(VTO=15.0 KP=8.63e-12 TOX=300e-9)

.ENDS  OFET
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combining current I_D' and V_{DS} according to (1). The resulting equivalent circuit is shown in Fig. 3(b).

The dependence of I_D on V_{GS} caused by the nonconstant mobility $\mu(V_{\mathrm{GS}})$ can also be modeled by a VCCS. The total current I_D can be described by

$$I_D = k(V_{\mathrm{GS}})I_D' \tag{5}$$

where I_D' is the current without mobility modulation, and k describes the nonlinear dependence of I_D on V_{GS}. This can be rewritten as

$$I_D = I_D' + \left[k(V_{\mathrm{GS}}) - 1\right] I_D' \tag{6}$$

where the second term on the right-hand side describes the additional current related to the mobility modulation effect. This additional current can be modeled by the subcircuit shown in Fig. 3(c). The subcircuit uses I_D' and V_{GS} as input variables and combines them according to (2).

The complete model whose netlist is given in Table I can be implemented in the PSPICE circuit simulator and requires only five additional parameters that can be extracted from the output characteristics. Comparing the measured and modeled curves in Fig. 1(b) and (c), all characteristics show an excellent agreement. In particular, in the range of $0 < |V_{\mathrm{GS}}| < 20$ V, where the charge carrier mobility significantly changes, the simulation results are in good accordance with the measurements, as shown in Fig. 1(d).

V. CONCLUSION

We have presented a simple PSPICE model for OFETs employing P3HT. This model is valid for P3HT transistors in the previously described configuration for gate voltage and drain voltage both ranging from 0 to -80 V. Different device capacitances directly affect the threshold voltage, whereas the series resistance influences the behavior of the field-effect mobility with the gate voltage. Furthermore, the mathematical approximations of G_{par} and μ allow for a flexible modeling of different curves.

This empirical model consists of the standard BSIM and two additional current sources. The underlying model equations extend the BSIM by only five additional parameters and allow for a simple parameter extraction. The correspondence between the behavior of the introduced parallel resistance and the charge carrier density in the numerical simulations confirms that the assumption of increased bulk conductivity with the gate bias is appropriate.

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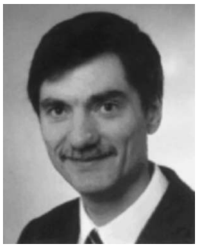

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