Understanding Strain-Induced Drive-Current Enhancement in Strained-Silicon n-MOSFET and p-MOSFET

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***Abstract*—Strain greatly affects the electrical properties of silicon because strain changes the energy band structure of silicon. In MOSFET devices, the terminal voltages induce electrical fields, which themselves modulate the electronic band structure and interact with strain-induced changes. Applied electrical fields are used to experimentally study different state-of-the-art local and global strain techniques and reveal the different responses of n- and p-MOSFETs to the different strain techniques. It is shown that p-MOSFETs have more low-lateral-field linear drive-current enhancement and less high-lateral-field saturation drive-current enhancement at both low and high vertical fields. The situation is similar for n-MOSFETs at low vertical fields. However, at high vertical fields, n-MOSFET low-lateral-field linear drive-current enhancement is less than the high-lateral-field saturation drive-current enhancement. The origin for this behavior can be found in the different strain effects on the electronic band structure, which results in effective mass reduction and/or scattering suppression. These, in turn, contribute differently to linear and saturation drive-current enhancements in n- and p-MOSFETs.**

***Index Terms*—CMOS, electrical field, MOSFET, mobility enhancement, SiGe, strain, strained overlayer film, strained silicon, strained silicon-on-insulator (sSOI), stress, stress memorization technique (SMT).**

I. Introduction

MOSFET scaling has been the main driver for the integrated circuit technology over the past decades. Intrinsic transistor delay has decreased continuously in accordance with a reduction in gate length, enabled by a reduction in the gate oxide thickness. From the 90-nm technology on, strained silicon channels were required to keep pace with Moore's law due to the inability to further scale the gate oxide thickness. Strain increases the effective carrier velocity in the channel, which compensates the detrimental effects of parasitic resistance and reduced voltage in short-channel devices [1].

These significant improvements of the transport properties in the strained silicon channel result in higher drive currents without gate oxide scaling, and, thus, strained silicon techniques have been rapidly adopted in the industry. Strain techniques are classified as local process-induced, such as stressed overlayers [2], [3], embedded source/drain stressors [4]–[8], stress memorization techniques (SMTs) [9]–[11], or stressed contacts and metal gates [12]. Strain can also be built directly into the substrate and is, thus, classified as globally strained [13], [14]. Table I gives an overview of the reported strain techniques and their benefits. The trends are consistent among the various stress techniques, showing that the drive current of short-channel p-MOSFETs in the low-lateral-field regime (low drain–source voltage V_{DS}, i.e., linear drain current) is enhanced more by local strain techniques than in the high-lateral-field regime (high drain–source voltage, i.e., saturation drain current) [6], [15]–[18]. In contrast, the corresponding ratio of linear versus saturation current benefit for n-MOSFETs tends toward unity or even less than unity [19], [20]. Beyond these observed trends, however, there is a lack of in-depth understanding of the physical factors that contribute to this behavior, in particular, the difference between n- and p-MOSFETs.

This paper is an experimental study of strain-induced drain-current enhancements from compressive and tensile overlayers, embedded SiGe, stress memorization, and global strain techniques [strained silicon-on-insulator (sSOI) substrates]. In contrast to reported data that are typically limited to specific saturation and linear current metrics at particular voltage conditions [15], [21], or studies with wafer bending techniques that impart strain independent of the strain technique [22]–[24], this paper focuses on the drive-current enhancement response of each strain technique as a function of applied vertical and lateral electrical fields. The MOSFET device terminal voltages are used to induce electrical fields that themselves modulate the electronic band structure and, thus, interact with strain-induced drive-current changes. The reaction of each individual stress technique to changing vertical and lateral electrical fields reveals the different behavior of n- and p-MOSFETs: Local and global strained n-MOSFETs exhibit similar behavior under changing vertical and lateral electrical fields, whereas strained p-MOSFETs show a different sensitivity resulting from the electronic band structure modulation caused by the particular strain processes.

This paper is organized as follows: In Section II, details of the process flow are addressed, and implementation of each strain technique is highlighted. In Section III, the impact of

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TABLE I
COMPARISON OF THE ENHANCEMENTS OF CARRIER MOBILITY $\Delta\mu$, SATURATION DRAIN CURRENT $\Delta I_{D,\mathrm{sat}}$ AND LINEAR DRAIN CURRENT $\Delta I_{D,\mathrm{lin}}$ FOR VARIOUS STRAIN TECHNIQUES WITH RESPECT TO UNSTRAINED DEVICES [6], [11], [19], [25], AND [26]. THE RATIO BETWEEN $\Delta I_{D,\mathrm{sat}}$ AND $\Delta I_{D,\mathrm{lin}}$ IS GREATER UNITY FOR n-MOSFETS, WHEREAS IT IS SMALLER UNITY FOR p-MOSFETS

	$\Delta\mu$ (%)	$\Delta I_{D,sat}$ (%) (V_{DS} = 1.0 V)	$\Delta I_{D,lin}$ (%) (V_{DS} = 0.05 V)	$\Delta I_{D,sat}$ / $\Delta I_{D,lin}$
n-MOSFET				
TOL [19]	28	18	11	**1.6**
SMT [11]	12	14	11*	**1.3**
sSOI [25]	50	10	–	–
p-MOSFET				
COL [26]	–	40	106	**0.4**
eSiGe [6]	50	25	50	**0.5**

* V_{DS} = 0.1 V

varying lateral and vertical electrical fields on the electrical characteristics of these strained devices is presented. Section IV discusses the relationship between carrier mobility enhancement and drain-current enhancement, and the physics behind the field dependence of the drain-current enhancements under strain from overlayer stressors. A comparison of the induced stress patterns resulting from the various strain techniques and their influence on the drive-current enhancements is examined. Finally, conclusions are drawn in Section V.

II. DEVICE FABRICATION

A variety of strained silicon MOSFET devices were fabricated on (001) silicon-on-insulator wafers with 38-nm physical gate length featuring 1.3 nm SiON as the gate dielectric and polysilicon as the gate material [15], [27]. The channel is oriented along the ⟨110⟩ direction. After shallow trench isolation, gate, and spacer formation, the embedded SiGe (eSiGe) process is implemented with epitaxial growth of SiGe in cavities etched into the source/drain areas of p-MOSFETs [21]. An SMT is implemented for n-MOSFETs [28] by the deposition of a dielectric stress film prior to the standard final activation anneal by means of rapid thermal annealing. After SMT-film removal, nickel silicide was formed. A highly strained tensile overlayer film (TOL) and a compressive overlayer film (COL) are deposited on n- and p-MOSFETs, respectively. The flow finishes with a standard back-end process. Each strained device was processed with only one of the aforementioned stressors to decouple the effects of each strain technique, and only beneficial stress techniques were studied for each polarity of MOSFETs, i.e., n-MOSFETs got an SMT or a TOL, and p-MOSFETs got eSiGe or a COL. For each case, a corresponding unstrained reference was coprocessed within the same lot.

In addition to the local stressors (eSiGe, SMT, TOL, and COL), globally strained substrates were also investigated. These sSOI wafers have a tensile biaxial stress of 1.3 GPa in the silicon film. Since this strain is not the optimum for the performance improvement of p-MOSFETs, we analyze sSOI wafers only for n-MOSFETs, where a clear strain-driven improvement is visible. These devices received optimized annealing and implantation conditions to account for the stress-dependent diffusion.

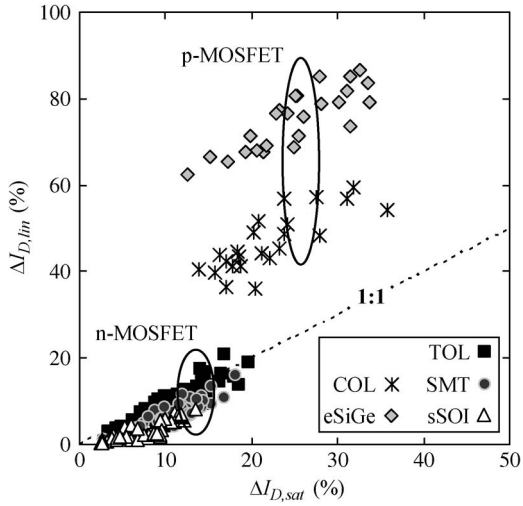

Fig. 1. Correlation between the change in drain current for linear ($V_{\mathrm{GS}} = 1.0$ V, $V_{\mathrm{DS}} = 0.05$ V) and saturation ($V_{\mathrm{GS}} = V_{\mathrm{DS}} = 1.0$ V) regimes originating from different strain techniques applied to n- and p-MOSFETs.

III. RESULTS

Drain-current enhancement ($\Delta I_D = (I_D^{\mathrm{strained}} - I_D^{\mathrm{unstrained}})/I_D^{\mathrm{unstrained}}$) from the various strain techniques is shown in Fig. 1. Linear ($V_{\mathrm{GS}} = 1.0$ V, $V_{\mathrm{DS}} = 0.05$ V) drive-current enhancement is plotted versus saturation ($V_{\mathrm{GS}} = V_{\mathrm{DS}} = 1.0$ V) drive-current enhancement for gate lengths ranging from 34 to 48 nm. The dotted line indicates identical linear $I_{D,\mathrm{lin}}$ and saturation drain current $I_{D,\mathrm{sat}}$ enhancement. There is a clear difference between the strained n- and p-MOSFETs. P-MOSFET linear drain-current enhancement $\Delta I_{D,\mathrm{lin}}$ is higher compared with saturation drain-current enhancement $\Delta I_{D,\mathrm{sat}}$ for the corresponding p-MOSFET stressors, eSiGe and COL. This relation is reversed for strained n-MOSFETs for the corresponding n-MOSFET stressors SMT, TOL, and sSOI. This is in agreement with the published data from Table I. In Fig. 1, there is also a much stronger improvement for p-MOSFET devices compared with those of n-MOSFETs. This is due to a combination of p-MOSFET stressors being available at higher stress levels compared with the less effective n-MOSFET stressors, as well as a higher strain sensitivity of p-MOSFETs compared with that of n-MOSFETs [29].

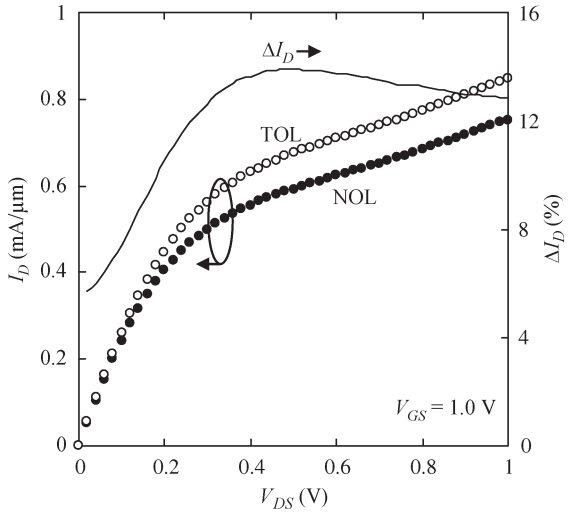

Fig. 2. Output characteristic of an unstrained and a TOL-strained n-MOSFET at $V_{\rm GS} = 1.0$ V. The stress-induced drain-current enhancement as a function of the drain–source voltage $V_{\rm DS}$ is also shown.

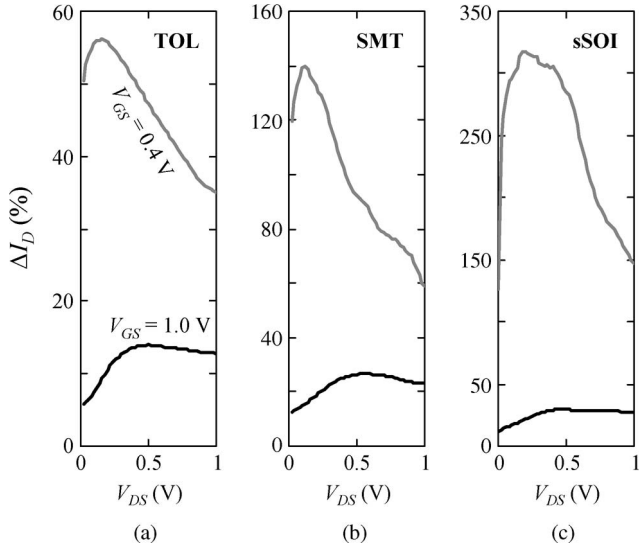

Fig. 3. Change in strain-induced n-MOSFET drain-current enhancements as a function of the drain–source voltage $V_{\rm DS}$ for different strain techniques: (a) TOL, (b) SMT, and (c) sSOI.

This difference in linear versus saturation drive-current enhancement ratio occurs at different lateral electrical fields, so their dependence on lateral as well as vertical electrical fields is analyzed in more detail in the following.

A. Lateral Electrical Field

1) n-MOSFETs: The output characteristics of n-MOSFETs with neutral (NOL) and tensile stressed nitride overlayer films (TOL) are shown in Fig. 2 as an example to illustrate drive-current enhancement versus lateral electrical field (proportional to the drain–source voltage $V_{\rm DS}$). The strain-induced drain-current enhancement is also plotted versus $V_{\rm DS}$ at the gate–source voltage $V_{\rm GS} = 1.0$ V.

The strain-induced drain-current enhancements at $V_{\rm GS} = 0.4$ V and at $V_{\rm GS} = 1.0$ V are plotted in Fig. 3 for all three strain techniques suitable for n-MOSFETs (TOL, SMT, and sSOI) versus the drain–source voltage. The value 0.4 V for $V_{\rm GS}$ was chosen to have a low vertical electrical field case but simultaneously ensure the formation of an inversion layer.

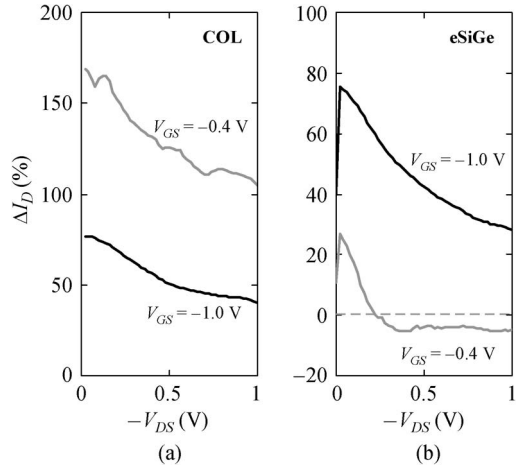

Fig. 4. Change in strain-induced p-MOSFET drain-current enhancement as a function of the drain–source voltage $V_{\rm DS}$ for different strain techniques: (a) COL and (b) eSiGe.

For $V_{\rm GS} = 1.0$ V and starting from low $V_{\rm DS}$, drain-current enhancement increases, saturates, and then decreases slightly at higher lateral fields. It is a similar trend for all stress cases and is consistent with all published data showing more saturation drive-current enhancement and less linear drive-current enhancement in n-MOSFETs. However, at a lower gate overdrive value of $V_{\rm GS} = 0.4$ V, this behavior changes significantly.

The stress-induced threshold voltage shift in the strained device also contributes (for a given gate overdrive) to the higher drain–current, as will be quantified in Section IV-B.

2) p-MOSFETs: For p-MOSFETs, two strain techniques have been investigated: the compressive strained nitride overlayer (COL) and the embedded SiGe (eSiGe). A higher lateral electrical field causes a lower drive-current gain for both p-MOSFET stressors, as shown in Fig. 4. Higher vertical fields $(V_{\rm GS} = -1.0$ V) also reduce the COL-induced drain-current enhancements compared with the low vertical field case $(V_{\rm GS} = -0.4$ V), but allow significantly enhanced drive-current gains for devices with eSiGe.

B. Vertical Electrical Field

1) n-MOSFETs: The effective vertical field is perpendicular to the channel and is controlled by the gate–source voltage. The linear and saturation transfer characteristics of n-MOSFETs with neutral and tensile strained nitride overlayer films are shown in Fig. 5 as an example. The strain-induced linear and saturation current is also plotted versus the gate–source voltage $V_{\rm GS}$. Generally, there is a reduction in the drive-current enhancement for higher vertical fields, consistent with the data presented in Figs. 3 and 4. There is a clear difference between linear and saturation drive-current improvement. In the subthreshold regime, the linear drive-current gain $\Delta I_{D,\rm lin}$ is significantly larger than the saturation drive-current gain $\Delta I_{D,\rm sat}$. This difference reduces for increasing gate–source voltages, and the curves cross near $V_{\rm GS} = 0.6$ V, where both

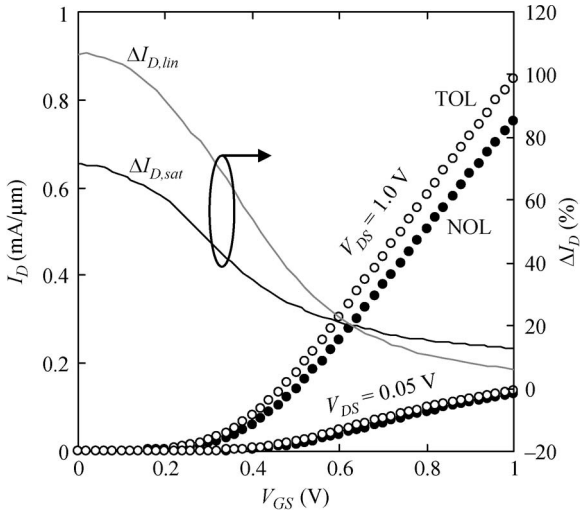

Fig. 5. Transfer characteristic for unstrained (NOL) and strained (TOL) n-MOSFET devices in linear ($V_{\rm DS} = 0.05$ V) and saturation ($V_{\rm DS} = 1.0$ V) regions. Also shown is the strain-induced I_D change.

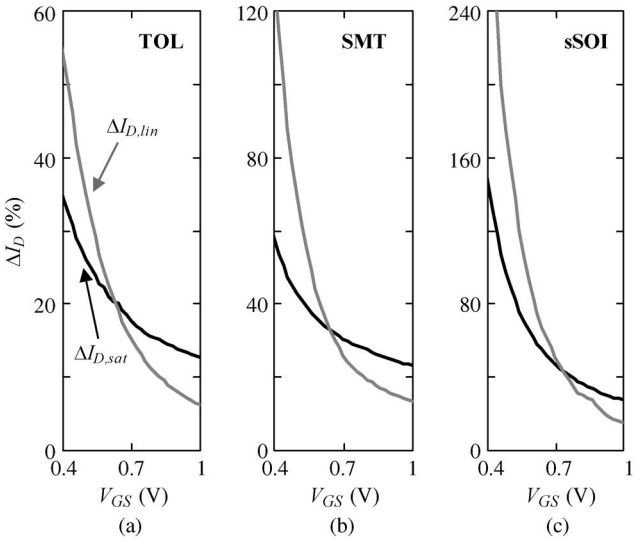

Fig. 6. Change in strain-induced n-MOSFET drain-current enhancement (for linear and saturation region, $V_{\rm DS} = 0.05$ V and $V_{\rm DS} = 1.0$ V, respectively) as a function of the gate–source voltage for different strain techniques: (a) TOL, (b) SMT, and (c) sSOI.

drive-current gains are identical. For even higher voltages, $\Delta I_{D,\rm lin}$ falls below the value of $\Delta I_{D,\rm sat}$.

Fig. 6 shows the vertical field (represented by the gate–source voltage) response of drain-current enhancement beyond the occurrence of inversion for TOL, SMT, and sSOI stressors. All stressors exhibit a similar behavior showing reduced drain-current improvement for higher vertical electrical fields. For small vertical fields, there is a higher gain in $I_{D,\rm lin}$ compared with $I_{D,\rm sat}$ and a reverse relation for high vertical fields.

2) p-MOSFETs: The drain-current enhancement for devices with eSiGe is shown together with that of COL devices in Fig. 7 and shows, again, a different behavior compared with the n-MOSFET case. The linear drive-current enhancement $\Delta I_{D,\rm lin}$ is larger than the saturation drive-current enhancement $\Delta I_{D,\rm sat}$ for all measured gate–source voltages. A decrease in

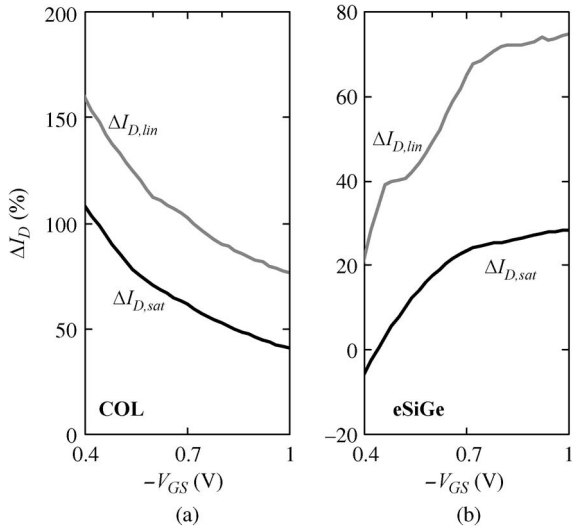

Fig. 7. Change in strain-induced p-MOSFET drain-current enhancements (for linear and saturation region, $V_{\rm DS} = -0.05$ V and $V_{\rm DS} = -1.0$ V, respectively) as a function of the gate–source voltage for different strain techniques: (a) COL and (b) eSiGe.

the drain-current gain (for both linear and saturation) for higher voltages is observed similar to n-MOSFETs in the case of COL, but in the case of eSiGe, the response to changes in the gate–source voltage is reversed, i.e., the drive-current gain increases with a higher gate–source voltage.

C. Combined Lateral and Vertical Electrical Fields

Fig. 8 shows the contours of drain-current enhancement versus lateral and vertical electrical fields. The three stressors for n-MOSFETs exhibit, as discussed above, similar electrical field dependence. For p-MOSFETs, the two stressors look quite different from each other. Whereas the COL-strained device has similarities with the n-MOSFET stressors, p-MOSFETs strained with eSiGe show a different behavior, which is, however, similar to the one described in [30]. At a higher gate bias, p-MOSFETs with an eSiGe stressor exhibit higher drive-current benefits in contrast to COL-strained p-MOSFETs, which show reduced enhancement at higher gate overdrive.

IV. Discussion and Analysis

A. Correlation Between Mobility and Drain-Current Enhancements

The fundamental relationship between low-field mobility and drive current in short-channel MOSFETs (sub-100 nm) is not well understood. This is because mobility is difficult to determine in short-channel devices, as intrinsic channel resistance cannot be easily distinguished from extrinsic source/drain resistance by measurement [31], [32]. Also, the uncertainty of the effective gate length aggravates these uncertainties [33]. Moreover, inversion charge density cannot be easily reached due to large parasitic gate capacitance [34]. However, low-field mobility is still of crucial importance to carrier velocity and,

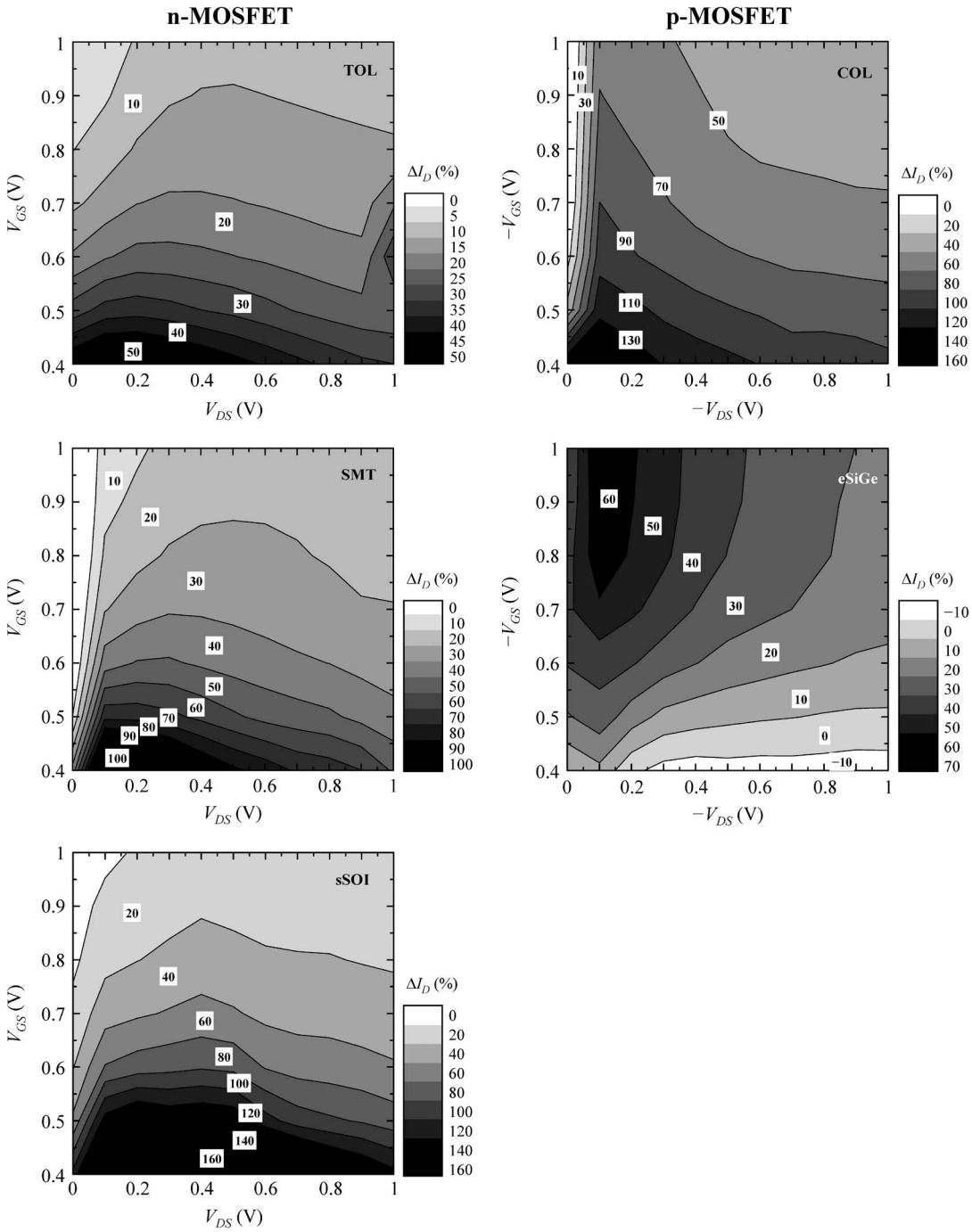

Fig. 8. Dependence of the strain-induced drive-current enhancement on the applied electrical field for various strain techniques in n- and p-MOSFETs.

hence, drive current in modern devices [35]. Although the exact value of mobility is difficult to determine, changes in mobility can be extracted more reliably [36].

For the following analysis, the transistor is described within a simple resistance model with the total resistance R_{total} comprising a series connection of the channel resistance R_{channel} and the parasitic external source/drain resistance R_{SD}, i.e.,

$$R_{\text{total}} = \frac{V_{\text{DS}}}{I_{D,\text{lin}}} = R_{\text{channel}} + R_{SD}. \tag{1}$$

After [19], the strain-induced change in $\Delta I_{D,\text{lin}}$ can be expressed as a function of the change in mobility $\Delta\mu$ and the change in parasitic source/drain resistance ΔR_{SD}, i.e.,

$$\Delta I_{D,\text{lin}} = \frac{R_{\text{channel}}^{\text{strained}}}{R_{\text{total}}^{\text{strained}}}\Delta\mu + \frac{R_{SD}^{\text{strained}}}{R_{\text{total}}^{\text{strained}}}\Delta R_{SD}. \tag{2}$$

Following further [19], $\Delta\mu$ can be expressed as

$$\Delta\mu = \frac{\mu^{\text{strained}} - \mu^{\text{unstrained}}}{\mu^{\text{unstrained}}} \approx \frac{R_{\text{channel}}^{\text{unstrained}} - R_{\text{channel}}^{\text{strained}}}{R_{\text{channel}}^{\text{strained}}}. \tag{3}$$

TABLE II
EXTRACTED PARASITIC SOURCE/DRAIN RESISTANCE R_{SD} USING THE dR/dL METHOD IN [36] FOR UNSTRAINED AND STRAINED TRANSISTORS

R_{SD} ($\Omega\cdot\mu$m)	n-MOSFET			p-MOSFET	
	TOL	SMT	sSOI	COL	eSiGe
Strained	216	190	376	379	342
Unstrained Reference	220			479	

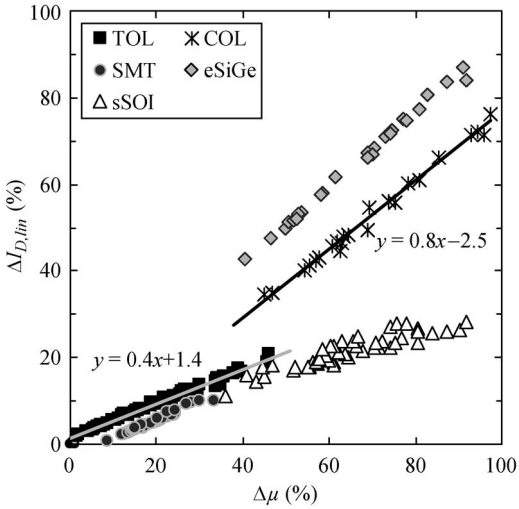

Fig. 9. Correlation between the carrier mobility change and the change in linear drain current for different strain techniques for n- and p-MOSFETs.

The change in parasitic source/drain resistance ΔR_{SD} was extracted using the dR/dL method [36]. The obtained values for R_{SD} are given in Table II.

The correlation between the strain-induced mobility change $\Delta\mu$ and the corresponding change in linear drain current $\Delta I_{D,\mathrm{lin}}$ is given in Fig. 9. Again, a clear difference for n- and p-MOSFETs is evident. The slope of the fitting curves shows that for n-MOSFET devices, a 50% change in mobility leads to a 20% change in linear drain current $I_{D,\mathrm{lin}}$. For p-MOSFETs, this relation is closer to unity, i.e., a 50% mobility improvement causes a 40% $I_{D,\mathrm{lin}}$ enhancement.

All n-MOSFETs exhibit the same slope for $\Delta I_{D,\mathrm{lin}} - \Delta\mu$ regardless of the applied strain technique, which agrees with the data from the previous sections (all n-MOSFET stressors behave similarly). The two p-MOSFET cases have the same slope but different offsets, which are caused by the reduced R_{SD} for eSiGe devices due to a lower contact resistivity originating from the lower SiGe valence band offset. For a small $R_{SD}/R_{\mathrm{channel}}$ ratio, the change in $I_{D,\mathrm{lin}}$ is dependent on $\Delta\mu$. For increasing the $R_{SD}/R_{\mathrm{channel}}$ ratio, the parasitic source/drain resistance change ΔR_{SD} is dominant.

At low lateral fields, MOSFET transport is limited by scattering mechanisms (Coulombic, acoustic phonon, and surface roughness) that are together characterized by μ_{eff}, such that the carrier velocity $v = E_{\mathrm{lat}} \cdot \mu_{\mathrm{eff}}$. An additional mechanism, i.e., optical phonon scattering, is not important at low lateral fields, but becomes dominant at higher lateral fields and increases proportionally to the electrical field leading to "velocity saturation" in long channels with high fields. However, in short-channel devices, carriers do not reach v_{sat} instantaneously. Instead, in the saturation regime, the carrier transport is more and more governed by ballistic transport [37]–[40]. Nevertheless, effective mobility (at low lateral fields) and carrier velocity are correlated in scaled MOSFETs [41], although there is no universal agreement about this correlation [42]. The change in $\Delta I_{D,\mathrm{sat}}$ can be expressed as [20]

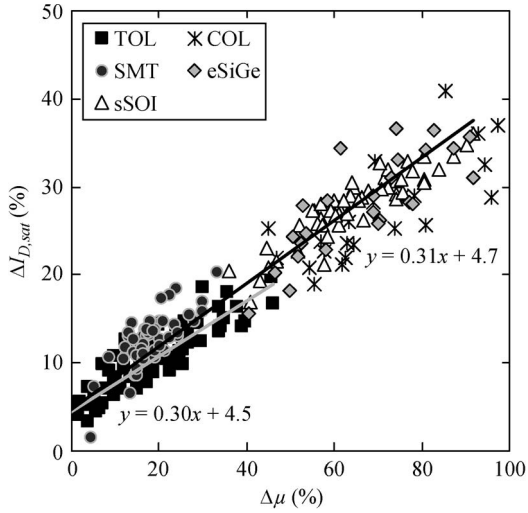

Fig. 10. Correlation between the carrier mobility change and the change in saturation drain current for different strain techniques for n- and p-MOSFETs.

$$\Delta I_{D,\mathrm{sat}} \approx (1 - B)\Delta\mu \tag{4}$$

where B is the ballistic efficiency.

Fig. 10 shows the $I_{D,\mathrm{sat}}$ benefit from each stressor. Both strained n- and p-MOSFET devices are located on a single curve with a similar slope for all strain techniques. The extracted B values are ~0.61 for n-MOSFETs and ~0.63 for p-MOSFETs. These values are at the upper limit of the typically reported range of 0.45–0.60 [19], [41], [43]. Equation (4) indicates that a 50% improvement in mobility causes a 20% enhancement in $I_{D,\mathrm{sat}}$ for n-MOSFETs, and for p-MOSFETs, this ratio is similar (50% to 22%).

The values of R_{SD} and R_{channel} are important for a correlation between $\Delta\mu$ and $\Delta I_{D,\mathrm{lin}}$ [see (2)], whereas for $\Delta I_{D,\mathrm{sat}}$, the parasitic source/drain resistance R_{SD} is of no relevance [cf. (4)]. As can be seen from Fig. 11, n-MOSFET devices have a worse $R_{SD}/R_{\mathrm{channel}}$ ratio. This is the reason why $\Delta I_{D,\mathrm{lin}}$ is much lower for given $\Delta\mu$ for n-MOSFETs compared with p-MOSFETs. The high $R_{SD}/R_{\mathrm{channel}}$ ratio for n-MOSFETs is not driven by a high R_{SD} (as can be seen in Table II), but rather by a very low channel resistance R_{channel} due to the higher electron mobility. This results in lower channel resistivity compared with p-MOSFETs. Although this difference is of importance for the low-field linear drive-current enhancement, it has almost no influence in the high-field saturation region where the ballistic efficiency B determines the drive-current enhancement for a given mobility gain. The different ratios of ΔI_D to $\Delta\mu$ for n- and p-MOSFETs with TOL and COL, respectively, are summarized in Fig. 12.

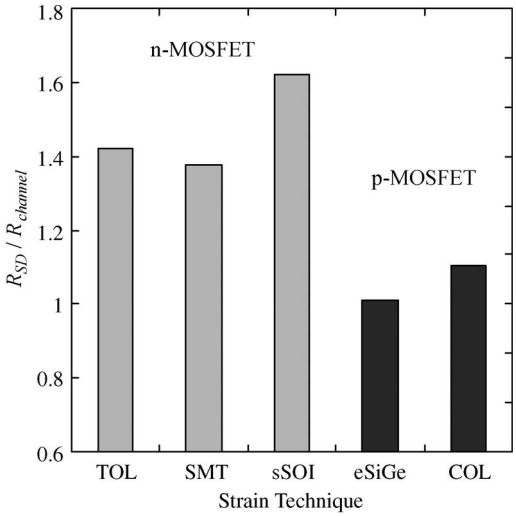

Fig. 11. Ratio of the parasitic source/drain resistance to the channel resistance for different strain techniques. All n-MOSFET devices have parasitic resistance higher than the channel resistance, whereas in p-MOSFETs, these two resistances are roughly equal.

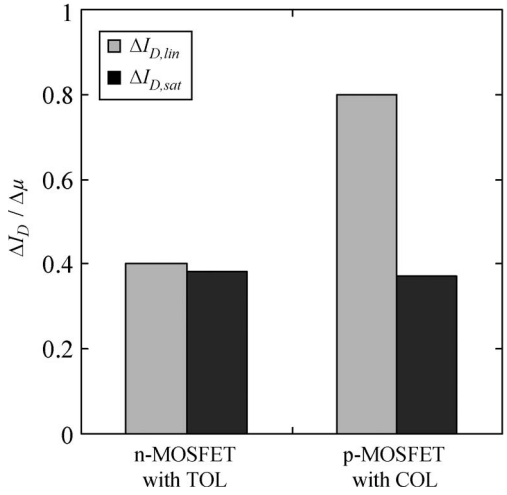

Fig. 12. Ratio of drain-current enhancement to mobility enhancement for n- and p-MOSFET devices with TOL and COL, respectively.

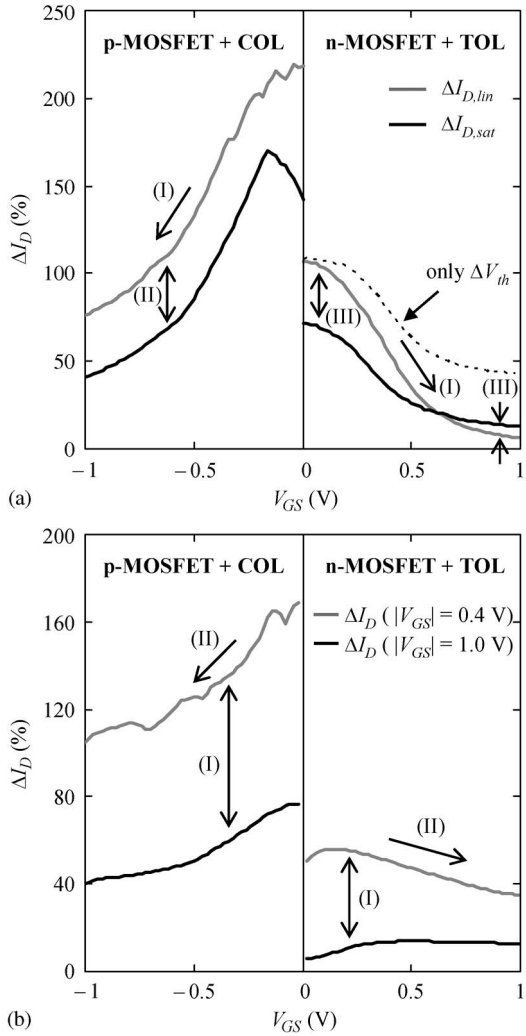

Fig. 13. Comparison of the drain-current enhancement for n- and p-MOSFETs for changing (a) vertical ($\propto V_{\rm GS}$) and (b) lateral ($\propto V_{\rm DS}$) electrical fields. N- and p-MOSFETs are strained by means of TOL and COL, respectively.

B. Detailed Analysis of Overlayer-Strained Devices

For the following discussion, only n- and p-MOSFETs with strained overlayer films (TOL and COL, respectively) are considered. This type of a stressor introduces stress into the device without changing other device parameters such as modified junction profiles due to stress-altered diffusion or embedding new materials with differing material properties compared with the unstrained reference. The observed change in electrical behavior can be attributed completely to the additional strain, which allows a fair comparison between strained and unstrained devices.

Fig. 13 summarizes the behavior of different electrical field conditions on the strain-induced changes in drive current for n- and p-MOSFETs. There are several effects.

I) For all cases (n- and p-MOSFETs as well as $I_{D,\rm lin}$ and $I_{D,\rm sat}$), there is a reduction in drain-current enhancement with higher vertical electrical fields ($\propto V_{\rm GS}$). Higher carrier scattering at the $\rm Si/SiO_2$ interface due to stronger confinement occurs for both unstrained and strained transistors. However, according to Matthiessen's rule, the contribution of the surface-roughness-limited mobility $\mu_{\rm SR}$ on the total mobility μ is higher in strained transistors due to the stress-driven increase in phonon-limited mobility $\mu_{\rm phonon}$. Furthermore, for strained n-MOSFETs, the preferential occupancy of Δ_2-valleys with thinner inversion layer thickness causes the electrons to be more prone to surface roughness scattering compared with the unstrained case. This results in lower improvements at higher vertical fields, where mobility is more governed by surface roughness scattering [44]. A similar effect is present for holes, where the surface scattering rate increases in strained p-MOSFETs due to the increasing population in the top subband. This results in the hole centroid being closer to the $\rm Si/SiO_2$ interface [45], [46].

The typical shape of the curves in Fig. 13(a) results, at least partly, due to the threshold voltage shift. Assuming two identical transfer characteristics, with one of them slightly shifted by several millivolts on the x-axis

compared with the other, the calculation of the "current enhancement" results in higher numbers in the subthreshold regime, reducing when passing over in the linear regime [dotted line in Fig. 13(a)].

II) As the lateral field increases, the stress-induced velocity gain, and, thus, the drain-current enhancement, decreases for n- and p-MOSFETs. This is because carriers are rapidly heated with increasing lateral fields, and their velocity saturates at a constant value, i.e., the saturation velocity. Also, a repopulation from low-transport mass to high-transport mass regions within the $\boldsymbol{k}$-space occurs for heated carriers, thus reducing mobility differences between unstrained and strained devices [47].

III) The crossover of $\Delta I_{D,\mathrm{lin}}$ and $\Delta I_{D,\mathrm{sat}}$ for n-MOSFETs at midlevel vertical electrical fields is, however, puzzling. For low vertical fields, the enhancement in linear drain current is higher than in saturation, and this correlation is reversed at high vertical fields. As quantum confinement already favors the population of Δ_2-valleys in the absence of strain fields, additional strain-induced band splitting between Δ_4- and Δ_2-valleys is not significant for further mobility enhancements in sub-50-nm devices at high vertical fields [45]. The nonuniform formation of the inversion channel in the saturation region, with higher vertical fields at the source side and lower effective vertical fields at the drain side ("pinch-off"), renders the aforementioned effect less relevant compared with the linear transport case, where the high vertical field appears in the entire channel. This is the reason why for n-MOSFETs at high vertical fields, $\Delta I_{D,\mathrm{lin}}$ is smaller than $\Delta I_{D,\mathrm{sat}}$ since the confinement effects dominate more in the linear transport regime.

For holes, this effect is not present since the quantization has minor influence [46]. The mobility and drive-current enhancement is mainly driven by a reduction in effective transport masses due to band warping and not solely by the repopulation of carriers, which, in turn, interact with the electrical-field-induced changes.

C. Comparison of Applied Strain Techniques

A comparison of the induced stress components that are generated by the different strain techniques was simulated (Fig. 14). Using SYNOPSYS Sentaurus TCAD software, 2-D finite-element simulations are performed to analyze the stress distribution in devices with various stress techniques. The simulator uses the plane-strain condition, in which the out-of-plane elongation is set to zero, which is a valid assumption for large-width transistors. Silicon was treated as an anisotropic elastic material. Simulation devices were constructed and calibrated in a full complementary metal–oxide–semiconductor process flow. The eSiGe mainly generates a lateral compressive stress (σ_{xx}). Overlayer stressors generate a strong vertical stress (σ_{yy}) and only a small lateral stress (σ_{xx}), at least in modern state-of-the-art transistors with small contacted-gate pitches. For that reason, there is almost no shear stress with TOL/COL. This is of relevance as discussed below. Assuming that the polysilicon gate is the stress source in the SMT [10], both σ_{xx} and σ_{yy} are present at a significant level. For biaxial strained sSOI substrates, the stress is, as expected, only in-plane (σ_{xx} identical to σ_{zz}), and the out-of-plane (σ_{yy}) component is zero.

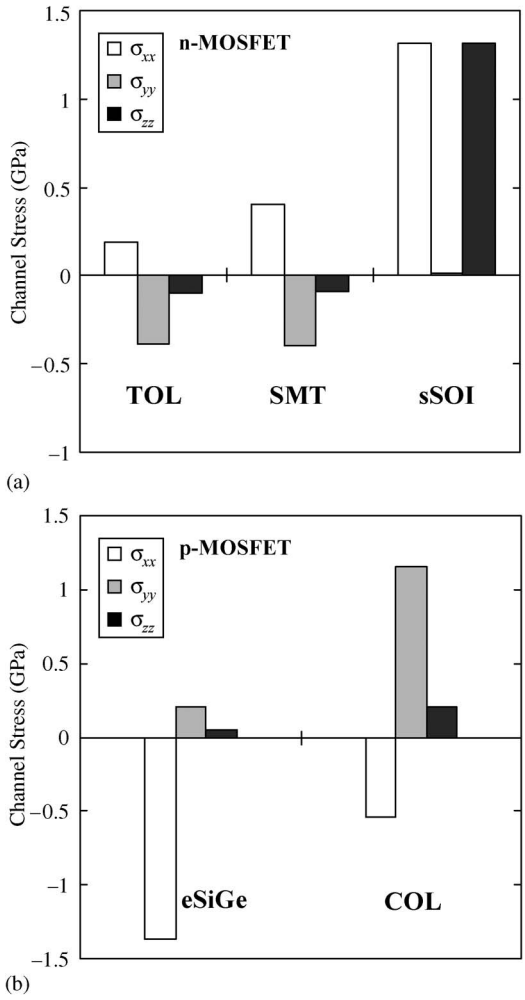

Fig. 14. Generated stress in the transistor channel induced from different strain techniques for (a) n-MOSFET and (b) p-MOSFET.

Since the electron enhancements for uniaxial and biaxial tensile strain arise from the same mechanism (namely, six-fold degenerate conduction band valleys split into two groups, i.e., Δ_2 and Δ_4), the electrical field dependence will also be identical. Thus, although the investigated n-MOSFET strain techniques induce a different stress pattern, their reaction on mobility is similar. This is summarized in Fig. 15, which shows the enhancement ratio of $\Delta I_{D,\mathrm{lin}}$ to $\Delta I_{D,\mathrm{sat}}$ as a function of the vertical field. The somewhat higher enhancements for sSOI n-MOSFETs can be related to an additional impact of the reduced surface roughness scattering in biaxial tensile strained inversion layers, as proposed by Fischetti *et al.* [48] and other groups [49], [50].

In case of p-MOSFETs, the hole mobility enhancement is strongly dependent on the applied stress pattern. The hole mobility gain from uniaxial lateral compression (i.e., eSiGe) results more from band warpage due to shear strain than from band separation as in the case of COL. Therefore, the linear drain-current enhancement is much larger for eSiGe than for COL. This is due to a lower effective transport mass, which is

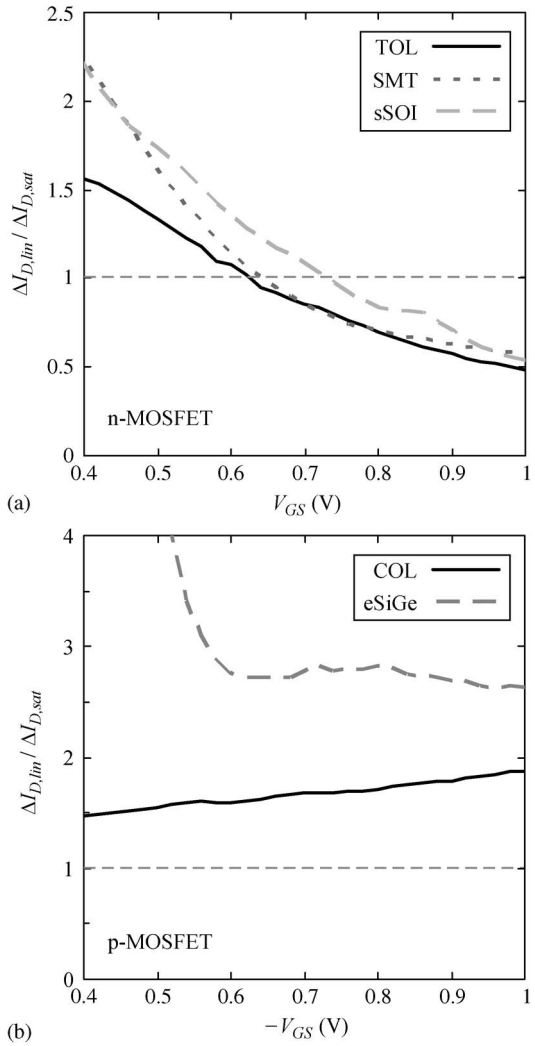

Fig. 15. Enhancement ratio of drain current in the linear regime to the saturation regime as a function of the vertical electrical field for (a) n-MOSFET and (b) p-MOSFET devices with different strain techniques.

important in linear transport. Also, the linear drive current is more sensitive to the reduced parasitic source/drain resistance of the SiGe regions. As it can be seen in Fig. 15, the $\Delta I_{D,\mathrm{lin}}$ to $\Delta I_{D,\mathrm{sat}}$ ratio is always larger than unity for both strain techniques and only shows marginal V_{GS} dependence. The majority of the mobility enhancement that holes experience from uniaxial strain is from the effective mass change rather than subband repopulation. This means that the subband repopulation caused by confinement has little impact on the response of the mobility to strain.

V. Summary and Conclusion

In addition to the efficiency of the strain techniques to enhance mobility and drive current, the overall device performance enhancement also depends considerably on the applied electrical field conditions inside the channel. Carrier quantization, saturation velocity effects, and carrier scattering at the $\mathrm{Si}/\mathrm{SiO}_2$ interface influence the carrier transport in MOSFETs and cause an attenuation of the desired strain effects compared with a bulk Si carrier transport case. Increasing lateral and vertical electrical fields generally cause a reduction of the strain-induced drain-current enhancements in both n- and p-MOSFETs. However, whereas for modern p-MOSFETs the low-field linear drive-current enhancements are higher than the high-field saturation drive-current enhancements for all studied vertical fields, the n-MOSFET shows this relation only for low gate–source voltages. At higher vertical fields, the strain-induced drive-current gain is lower in the linear region compared with the saturation region. This is independent of the applied stress patterns resulting from different strain techniques.

While it would be advantageous from the perspective of strain-induced drive-current enhancement to operate MOSFETs in the low electrical field range, high electrical fields are necessary to obtain drive high currents. Also, increasing channel doping density is needed to keep electrostatics in planar-geometry short-channel devices under control. The high electrical fields and resulting low mobility enhancements that inversion carriers experience in MOSFETs can be seen as a detrimental but inevitable side effect of device scaling. Therefore, the usefulness of strained silicon in future technology nodes lies in its ability to fundamentally alter the band structure in ways that enhance carrier transport even under high electrical fields, i.e., increase mobility through reduced effective transport mass and increased injection velocity in quasi-ballistic and ballistic MOSFETs rather than scattering suppression by carrier repopulation.

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