Rigorous Determination of CMOS Inverter Propagation Delay Time by TCAD

T. Herrmann[1], T. Feudel[2], J. Hoentschel[2], M. Horstmann[2], W. Klix[1] and R. Stenzel[1]

[1] University of Applied Sciences Dresden, Department of Electrical Engineering,
Friedrich-List-Platz 1, D-01069 Dresden, Germany
email: tom.herrmann@et.htw-dresden.de; tel.: +49 351 4622692; fax: +49 351 4622193

[2] AMD Saxony LLC & Co. KG, Wilschdorfer Landstrasse 101, D-01109 Dresden, Germany

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The switching speed of high performance CMOS transistors is often measured with ring oscillators in form of serial connected single inverters. The improvement of the transistors is reflected in a shorter propagation delay time of the inverters and those in a higher oscillation frequency of the ring oscillator. A very accurate and time consuming way of determining the oscillation frequency numerically by technology CAD (TCAD) is a mixed mode simulation of the whole ring oscillator. Another way is the extraction of the equivalent circuit elements out of the device simulation with a following circuit simulation. Such simulations are not effectively, if a lot of simulations have to be done during a device optimization. In this paper, the extracted propagation delay times of single inverter mixed mode simulations were compared with often used and less time consuming device simulations of single transistors and the simple CV/I approach. Their accuracy and usability will be shown for the design process of SOI CMOS FETs with gate lengths ranging from 65 nm down to 25 nm, which is comparable with the technology nodes described in [1].

The mixed mode simulation is a linked device and circuit simulation at every time step. It is used for combined simulation of n- and p-MOSFET and other devices like resistors or capacities as shown in Figure 1. If only one inverter is used, the next stage of the inverter chain could be modeled with a load capacitance [2]. Also single n- and p-MOS transistors charging and discharging a capacitive load can be simulated. The extracted propagation delay time is the time between reaching $V_{DD}/2$ at the input and output node. Here, the simulations were done with DIOS and DESSIS from the Synopsys TCAD suite [3]. The CV/I approach [4] takes the load capacitance multiplied with the half operating voltage and divided by the drive current. This formula did not account for any inner capacitances.

Figure 2 shows the results of the different methods for determining the propagation delay time at various load capacitances. The CV/I values are the lowest because the discharge of the capacitance started at $t = 0$ and the characteristic of the output voltage is linear approximated. Single transistors with a load capacitance have a propagation delay time between the inverter and the CV/I approach. Here, the discharge of the drain capacitance leads to a voltage overshoot at the load capacitance. Furthermore the lowering of the drain-to-source voltage during discharge of the load capacitance causes a lower current and a non linear behavior. The inverter is slowest due to its complexity. The appearing voltages could be seen in Figure 3. A propagation delay time of 4-5 ps is in the range of measured values. If

no load capacitance is used, the intrinsic propagation delay time is about 1.7 ps. A load capacitance of 3 fF takes into account the capacitances of the transistors and is therefore a good value to compare the different determination methods.

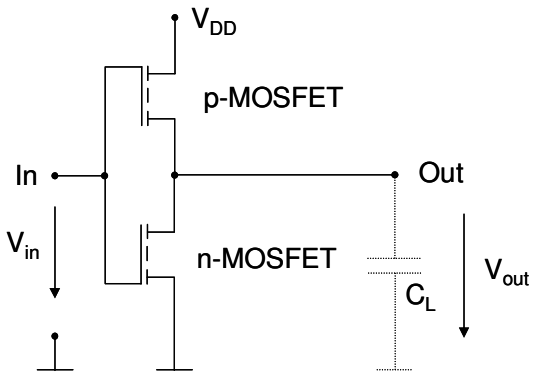

Figure 1: Inverter with load capacitance

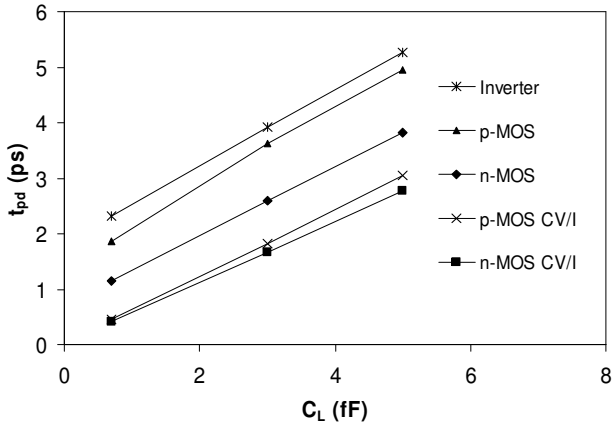

Figure 2: Propagation delay time vs. load capacitance for different approaches

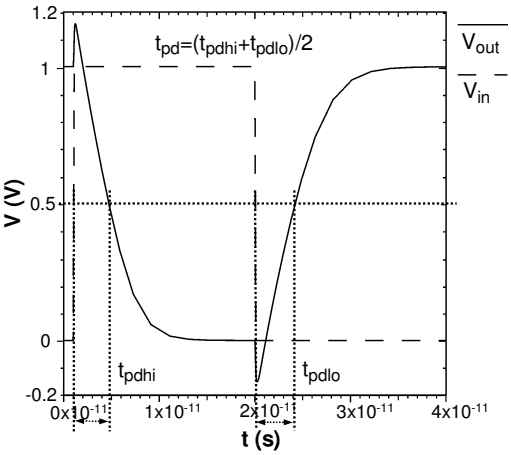

Figure 3: Input and output voltage of an inverter

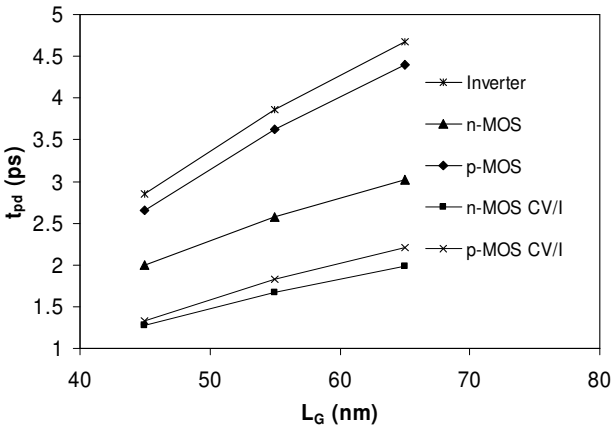

Figure 4: Propagation delay time vs. gate length for different approaches

Figure 4 shows the lowering of the propagation delay time for shorter gate lengths also for the different examination methods. The results show the underestimation of switching times by the simplified methods. The CV/I method could be slightly improved by adding the propagation delay time of a transistor without load to consider the inner capacitances.

Process- and device simulation of a CMOS inverter structure with a very short gate length L_G = 25 nm and an advanced non-diffusing doping profile results in an intrinsic propagation delay time of 0.9 ps and t_{pd} = 2.5 ps with 3 fF capacitive load.

[1] ITRS 2003 and ITRS 2004 update

[2] M.-E. Arbey, S. Galdin, P. Dollfus, P. Hesto, Proc. Eur. Solid-State Device Res. Conf., Stuttgart, 1997, p. 267

[3] DESSIS and DIOS Manual Release 10.0

[4] M. Bohr, Semiconductor International, 18 (1985), p. 75