Novel Approaches to Improve Laser Annealed SOI-MOSFETs

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Abstract

Laser anneal (LA) is one of the promising technologies for the 65 nm technology node and below. Steep and shallow junctions with a high level of activated dopants are fabricated by using Laser irradiation. The short time at high energy prevents diffusion in the extension and in the poly silicon gate. However, this causes extension underlap and poly depletion. Another problem might be the high extension sheet resistance due to the shallow junctions, despite of higher doping activation. We show a degradation of the universal curve ($I_{D,off}/I_{D,sat}$) for devices with LA in experiments and simulations. An analysis of the possible factors, which are responsible for the universal curve degradation is done by numerical simulations. Adjusting the threshold voltage by reducing the halo implantation dose improves the universal curve significantly. We have found an increase in saturation current of about 27% at the same off-state current and a gate delay improvement of the optimized transistor devices. Other approaches like deeper source and drain extensions to minimize the sheet resistance or a tilted source and drain extension implantation to get more overlap did not affect the universal curve significantly. Furthermore, we have investigated approaches to overcome the problems of laser annealed MOSFETs, which are easy to integrate into the current CMOS process.