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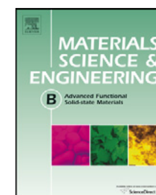

Gate length scaling trends of drive current enhancement in CMOSFETs with dual stress overlayers and embedded-SiGe

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ABSTRACT

Strain engineering in MOSFETs using tensile nitride overlayer (TOL) films, compressive nitride overlayer (COL) films, and embedded-SiGe (eSiGe) is studied by extensive device experiments and numerical simulations. The scaling behavior was analyzed by gate length reduction down to 40 nm and it was found that drive current strongly depends on the device dimensions. The reduction of drain-current enhancement for short-channel devices can be attributed to two competing factors: shorter gate length devices have increased longitudinal and vertical stress components which should result in improved drain-currents. However, there is a larger degradation from external resistance as the gate length decreases, due to a larger voltage dropped across the external resistance. Adding an eSiGe stressor reduces the external resistance in the p-MOSFET, to the extent that the drive current improvement from COL continues to increase even down the shortest gate length studied. This is due to the reduced resistivity of SiGe itself and the SiGe valence band offset relative to Si, leading to a smaller silicide-active contact resistance. It demonstrates the advantage of combining eSiGe and COL, not only for increased stress, but also for parasitic resistance reduction to enable better COL drive current benefit.

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1. Introduction

One of the most important challenges in developing ULSI technology today is to shrink device sizes in order to increase density. However, conventional gate length scaling based on shrinking the gate-oxide thickness has slowed down rapidly due to high gate leakage. Thus, strained silicon technology, based on process-induced stressors such as strained overlayers, stress memorization, and embedded-SiGe (eSiGe), has emerged as the key feature in CMOS technology. Strained silicon technology provides substantial drive current improvement without further gate length reduction.

With the continued march of Moore's law however, the stressors themselves have to be scaled. For future technology nodes, the scalability potential of stressors like strained nitride overlayer films [1,2] or embedded source/drain materials [3,4] is still under investigation. This fact stems from the tradeoff between two competing effects: smaller devices are easier to strain but the smaller volume of the stress-inducing material generates less stress. The parasitic source–drain resistance could be identified as another factor limiting the device's performance when the technology is scaled [5]. This work investigates the effect of gate length scaling by experiments and simulation of a strained silicon technology.

2. Device fabrication

n- and p-MOSFET were fabricated on SOI wafers using SiON as gate dielectric and polysilicon as gate material. After the formation of junction and silicide, different nitride films have been deposited on top of the devices in order to modulate the device performance. Transistors with strained overlayer films featuring various layer thicknesses and intrinsic film stresses (tensile and compressive for n- and p-MOSFET, respectively) were processed together with unstrained reference transistors using a neutral overlayer film. All other process parameters were identical. Furthermore a set of p-MOSFETs was processed with and without eSiGe. Details of the fabrication process can be found in Ref. [6].

3. Modeling

Finite-element simulations using SYNOPSYS Sentaurus TCAD software [7] have been employed to clarify the observed experimental behavior. Using measured SIMS profiles, TEM cross-sections

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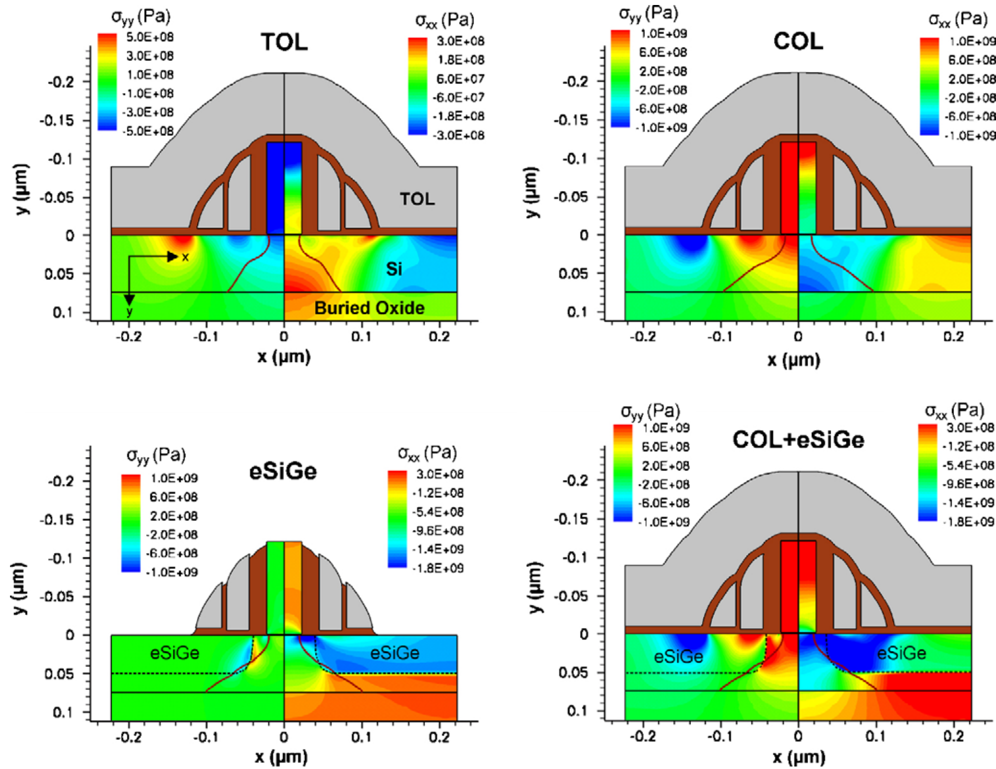

Fig. 1. Vertical (left part of each figure) and horizontal (right part) stress contour maps of a strained n-MOSFET with a tensile nitride overlayer (TOL) film as well as strained p-MOSFETs with a compressive nitride overlayer (COL) film, with eSiGe, and with a combination of both COL and eSiGe (positive values indicate tensile stress, negative values are compressive).

and transfer and output characteristics simulation devices were constructed and calibrated in a full CMOS process flow. A three-stream diffusion model [7] was used to simulate the dopant diffusion. The mechanical stress in the device is computed from the given initial stress in the layer, the material elastic constants, and the fabrication process steps. Any impact of the stress fields on the dopant diffusion and activation was neglected because the strained nitride layer is deposited after the final activation process. No further diffusion under stress occurs. Devices with different strained overlayer films have the same dopant profiles, meaning only stress fields have impact on electrical behavior. For the electrical device simulations, the hydrodynamic transport model was used assuming a constant saturation carrier velocity. The obtained stress distribution from mechanical simulations is transformed into carrier mobility change using strain-dependent mobility models for holes and electrons [7] in conjunction with the deformation potential model [8].

Fig. 1 shows the simulated device structure and compares the stress contour maps for the different strained MOSFETs. The simulations were done in 2D, which is sufficient for devices with a large gate width as the plane strain condition applies. For example, in the case of a n-MOSFET with tensile overlayer (TOL) a horizontal tensile stress (~200 MPa) and vertical compressive stress state (−400 MPa) arise in the channel region, the latter being mainly responsible for the performance improvement. In p-MOSFET devices it is observed from the simulations that the stress changes from either the COL or the eSiGe add up linearly to each other when combined.

4. Results and discussion

Mechanical stress induced by nitride layers greatly affects the performance of n- and p-MOSFETs. This is shown experimentally in Fig. 2, where drain-current enhancement versus an unstrained device ($\Delta I_{on}/I_{on} = (I_{on}^{strained} - I_{on}^{unstrained})/I_{on}^{unstrained}$) is plotted at constant off-current for various levels of channel stress. The channel stress is modulated by the stressed overlayer film properties, represented as the product of stress and thickness of the film. Increasing thickness of the overlayer or increasing intrinsic stress show a linear increase in drain-current improvement. There is no saturation visible in the investigated range. The somewhat steeper slope for the curve of the devices with compressive overlayer (COL) suggests that the p-MOSFET is more sensitive to stress than n-

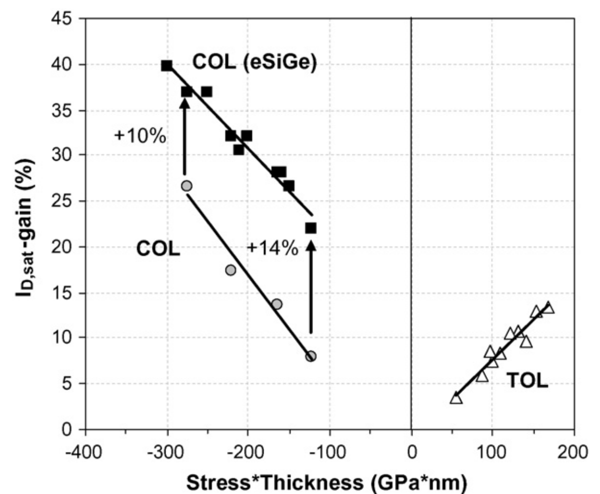

Fig. 2. Drive current enhancement from stressed overlayer films (compressive "COL" and tensile "TOL") compared to an unstrained device (L_G = 40 nm) at constant off-current. For "COL (eSiGe)" both splits, strained and reference, have eSiGe. The solid curves represent trend lines.

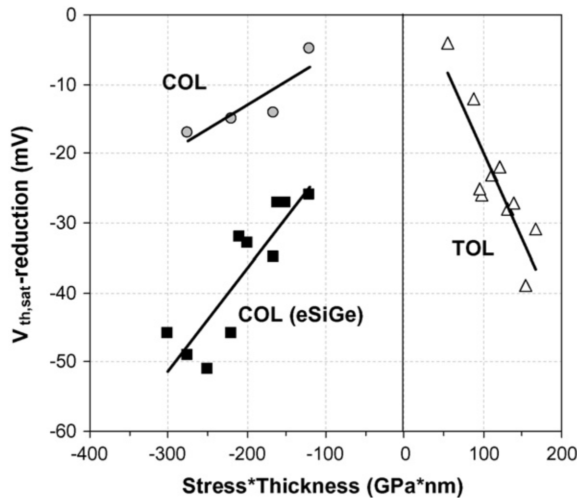

Fig. 3. Reduction of threshold voltage (absolute values for p-MOSFET) for various strained nitride overlayer films. The solid curves represent trend lines.

MOSFET. Comparing the p-MOSFET with eSiGe and neutral liner to a p-MOSFET with eSiGe and compressive liner ("COL (eSiGe)") there is a much higher improvement visible (up to 40%) which will be discussed later.

It should be mentioned, that the observed threshold voltage reduction (see Fig. 3) comes from strain-induced bandgap modulation. p-MOSFET exhibits less threshold voltage shift than n-MOSFET as also predicted by the deformation potential theory [8].

To investigate the gate length scaling behavior of strained nitride overlayer films, the drive current enhancement of a strained n-MOSFET was plotted versus gate length (Fig. 4). The drive current increases first with decreasing gate lengths, saturates for mid-length devices at around 70 nm and actually decreases with further reduction in gate length. This roll-off effect was investigated by 2D process and device simulations which were indeed able to reproduce this behavior (Fig. 4). The reasons for the roll-off are not obvious but could be separated by simulation data and are explained below.

The strain present in the Si-channel at the Si/SiO_2 interface (the location of the inversion layer) is analyzed first since it is predominantly responsible for the mobility enhancement which leads to drive current benefit of the device. As can be seen from Fig. 5, both stress components in the channel, horizontal and vertical one, increase in absolute values with decreasing gate length.

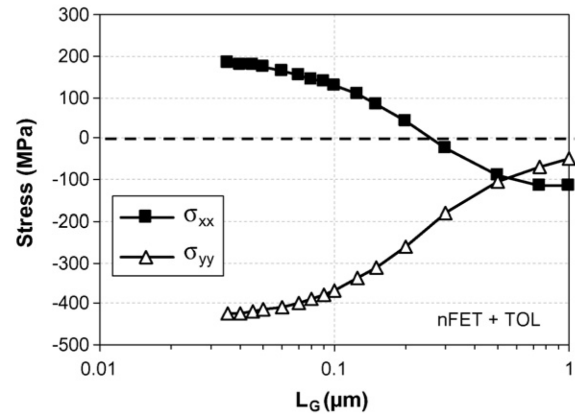

Fig. 5. Average stress, as obtained from mechanical simulations, along the transistor channel for n-MOSFET with tensile overlayer (taken 2 nm below the surface).

This is expected because the smaller volume of the wedged channel region in a scaled device can be more easily strained by the overlayer film. This increased strain results in increased carrier mobility and should also improve drive currents. However, for devices with sub-100 nm gate lengths, another effect emerges which counteracts the stress-benefit. The voltage dropped across the external resistance can no longer be neglected for such reduced gate lengths resulting in a loss in drive current. This effect could be capture with a simple model assuming a series connection of the channel resistance $R_{channel}$ and the external resistance R_{ext} comprising

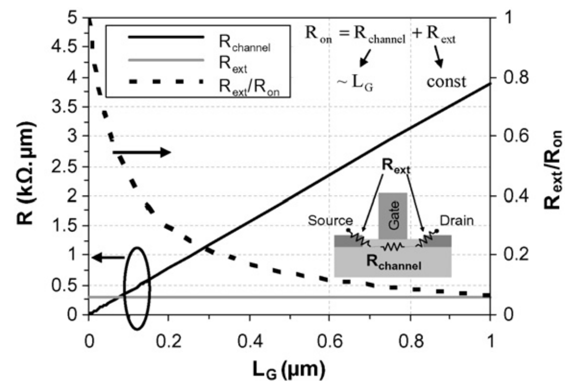

Fig. 6. Gate length dependence of the resistance components.

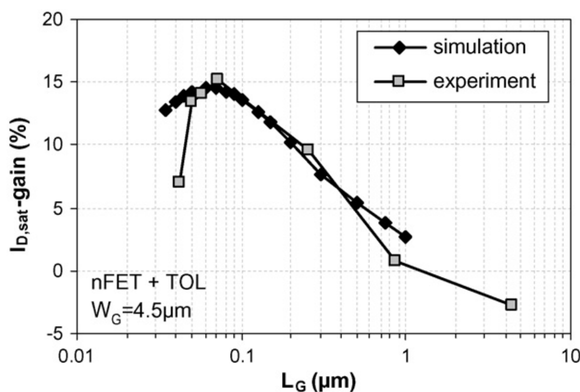

Fig. 4. n-MOSFET drain-current enhancement as a function of the gate length for a 100 nm thick tensile stressed overlayer with 1.2 GPa intrinsic stress. The device reference is with neutral liner. Also shown is a comparison to simulation data.

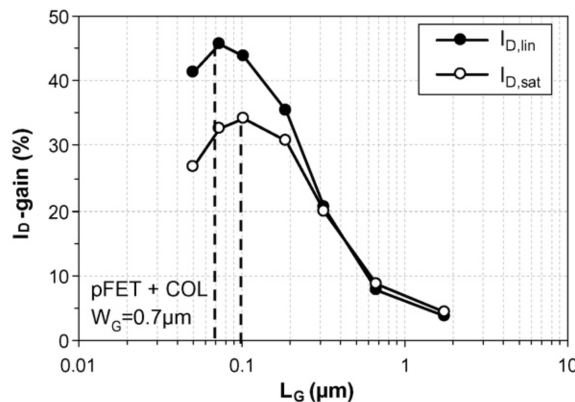

Fig. 7. p-MOSFET drain-current enhancement as a function of the gate length for a 100 nm thick compressive stressed overlayer with −2.5 GPa in linear regime (V_{DS} = −0.05 V, V_{GS} = −1.0 V) and saturation (V_{DS} = V_{GS} = −1.0 V).

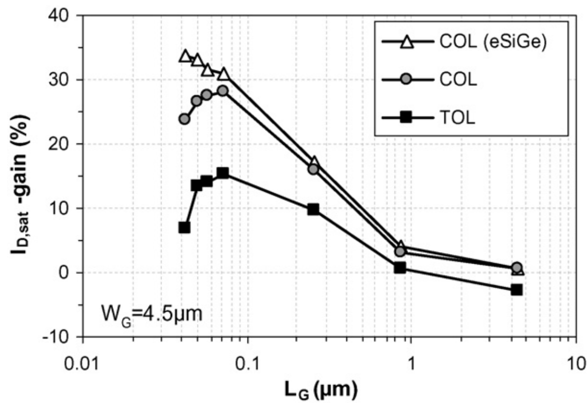

Fig. 8. Comparison of the drain-current enhancements for n-MOSFET with TOL, p-MOSFET with COL, and p-MOSFET with COL and eSiGe (for both, strained and reference devices).

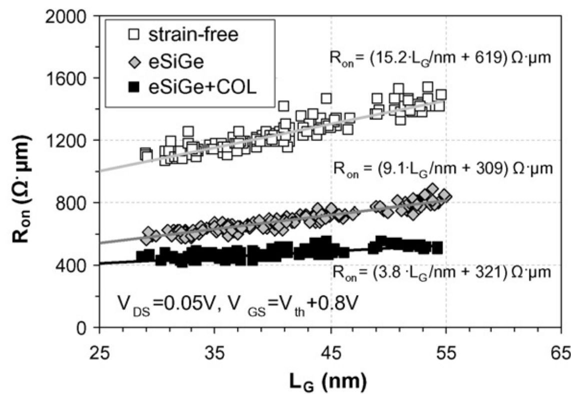

Fig. 9. p-MOSFET on-state resistance measurement at constant overdrive vs. L_G showing mobility and resistance improvement (slope reduction of the solid trend lines is an indication of channel mobility enhancement).

the on-resistance $R_{on} = R_{channel} + R_{ext}$. With a variation of the gate length, the channel resistance changes ($R_{channel} = \rho L_G/A$), but the external resistance remains nearly constant [9]. Fig. 6 shows the fraction of the external resistance to the total resistance (R_{ext} was determined as the intercept of L_G–R_{on} curve to a constant value of ~280 Ω μm). It can be seen that for short gate lengths, the influence of external resistance on the total resistance increases rapidly. Strain itself causes $R_{channel}$ to decrease but the components that make up the source–drain resistance are not changing significantly. Thus, the impact of the improved $R_{channel}$ on the overall device drive current diminishes for very short gate lengths, i.e. the strain-induced performance benefit is masked by the parasitic resistance for devices with gate lengths shorter than 70 nm.

A similar behavior could be seen for p-MOSFET devices with a compressive overlayer (Fig. 7). However, in the linear current regime, the roll-off curve changes due to the reduced effect of external resistance at lower voltage, providing higher improvements in $I_{D,lin}$ than in $I_{D,sat}$ for short gate lengths.

For p-MOSFET devices the possibility to add an eSiGe stressor is promising since it shows impressive drive current improvements itself [6]. In addition, the eSiGe stressor alters the drive current improvement behavior in the presence of a compressive overlayer, as shown in Fig. 8. In contrast to the drive current roll-off, here the drive current improvement continues to increase down to the shortest gate lengths studied. The reduced resistivity of the SiGe alloy, and a smaller contact resistance from a barrier height reduction due to the smaller bandgap of the SiGe alloy [10], add up to a greatly reduced source–drain series resistance as can be estimated using the dR/dL method in Fig. 9. This shifts the detrimental effect of the parasitic resistance to lower gate lengths which allow strain-induced benefits in $R_{channel}$ to significantly improve device performance even down to gate lengths below 30 nm.

The combined implementation of compressive overlayer and eSiGe shows clearly an advantage, not only in increased stress, but also for parasitic resistance reduction to enable better compressive overlayer drive current benefits.

5. Conclusion

Devices utilizing stressed nitride overlayers have the advantage of increasing mobility for shorter gate lengths resulting in increased drive currents. The drive current increases for decreasing gate length down to a critical gate length of 70 nm. Below this gate length, the external resistance starts to dominate the total resistance, and mobility gains have less impact on drain-current. This leads to reduced drain-current improvements despite increasing stress, as confirmed by process and device simulations. A simple model proves the increased influence of non-strain sensitive external resistance for smaller gate length. For p-MOSFETs combining compressive overlayers with eSiGe, the gate length where strain-induced drive current improvement begins to decrease could be suppressed down to 30 nm. The two times lower contact resistance of the SiGe material keeps the strain-dependent channel resistance as the dominant component of the total resistance, demonstrating that external resistance improvement is key to further scaling of strained silicon technologies.

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