Power handling limits in AlGaN/GaN large–scale RF–HEMTs

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Abstract

THE high breakdown field in GaN has launched excessive research on $AlGaN/GaN$ RF-power HEMTs during the past years. They promise higher power densities compared to $GaAs$ FETs at elevated operating voltages. However, as device maturity has allowed to demonstrate large-scale devices, the heat removal has tured out to limit the absolute RF-power. Whereas small devices have shown excellent power densities of $9.1\,W/mm$ in X-Band [1], larger devices show significantly reduced power densities [2].

We have simulated by a three-dimensional numerical solution of the heat flow equation the thermal impedances of devices with different layout and size both on SiC and sapphire substrates. It is shown that for gate-gate distances Δ_{gg} below $60\,\mu m$ strong thermal coupling between the channels takes place, leading to increased channel temperatures. For sapphire substrates, a thick Au-metallization can act as effective heat spreader, removing the heat from the critical channel region into the contact region and thus lowering the channel temperature. The same is valid for the GaN buffer layer with a typical thickness of $3\,\mu m$ and a high thermal conductivity of $130\,W/Km$ compared to the sapphire substrate ($\lambda \approx 50\,W/Km$). These effects can reduce the thermal impedance of $AlGaN/GaN$ HEMTs grown on sapphire considerably. Therefore, the thermal impedances of identical devices on sapphire and SiC ($\lambda \approx 500\,W/Km$) do not show the expected ratio of 10 but only 3–5 (fig. 1). Only for large devices, the thermal advantages of SiC substrates can be fully explored.

The comparison of simulated thermal impedances of 2-finger FETs with measured RF power densities at $2\,GHz$ shows decreasing power densities with increasing thermal impedances (fig 2). Therefore, the thermal impedance is a very critical device parameter that has to be minimized. Thermal coupling to the heatsink as well as the effect of substrate thinning will also be addressed.

References

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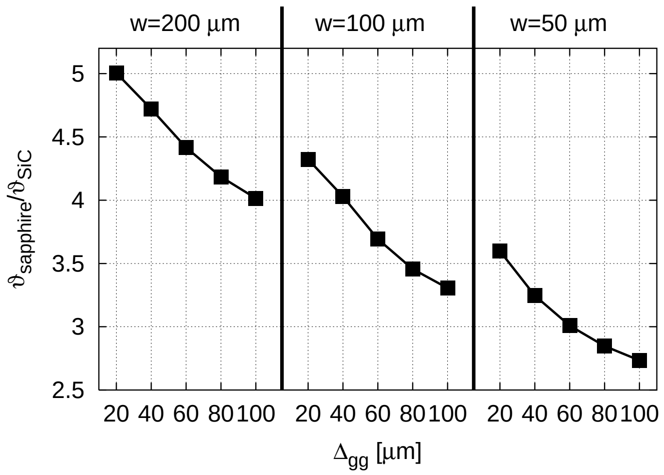

Fig. 1. ratio of thermal impedances of 4-finger-devices on sapphire and SiC substrates; gate-drain distance: $2\,\mu m$, buffer thickness: $3\,\mu m$, air-bridge Au-metallization thickness: $3\,\mu m$, substrate thickness: $300\,\mu m$; mesa width denoted by w and gate-gate distance by Δ_{gg}; The superior thermal properties of SiC substrates can only be explored in large devices.

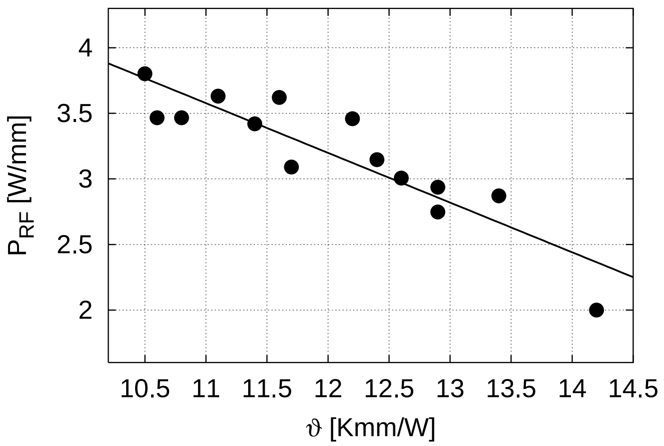

Fig. 2. measured RF-power at $2\,GHz$ plotted vs the simulated thermal impedance of several 2-finger FETs with different geometries.