Implementation and Optimization of Asymmetric Transistors in Advanced SOI CMOS Technologies for High Performance Microprocessors

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Abstract

Sub-40nm Lgate asymmetric halo and source/drain extension transistors have been integrated into leading-edge 65 nm and 45 nm PD-SOI CMOS technologies. With optimization, the asymmetric NMOS and PMOS saturation drive currents improve up to 12 % and 10 %, respectively, resulting in performance at 1.0 V and 100 nA/µm IOFF of NIDSAT = 1354 µA/µm and PIDSAT = 857 µA/µm. Product-level implementation of asymmetric transistors showed a speed benefit of 12 %, at matched yield and improved reliability.

Introduction

It has become extremely challenging for EOT scaling to keep pace with gate length reduction in advanced technology generations. This has resulted in non-optimal transistor electrostatic integrity, performance, and reliability tradeoffs. At a given EOT, however, a transistor with an asymmetric channel configuration can offer several advantages in terms of performance and electrostatics (1-4). This paper demonstrates that optimized transistors with asymmetric halos and asymmetric source/drain extensions can simultaneously improve drive current, reduce DIBL, reduce drain-side Miller capacitance, and reduce drain-side electric field. Optimized asymmetric transistors have been implemented on the product level, resulting in a substantial overall performance and reliability advantage.

Asymmetric Transistor Physics and Results

Fig. 1 shows a simulated doping profile of an asymmetric NMOS transistor with source-side-only halo and source-side tilted extension implantation. It is clear that there is more overlap of the source-side extension, less overlap on the drain side, and the halo creates a more abrupt junction on the source side while leaving a graded junction on the drain side.

Separating the effects of the asymmetric halo from the asymmetric extension, Fig. 2 shows that the source-side only halo increases the electric field near the source side for better carrier injection velocity. At the same time, the source-side-only halo creates a graded drain-side junction for lower electric field. These effects result, respectively, in improved drive current, as shown in Fig. 3, and reduced DIBL as shown in Fig. 4. The reduced DIBL is a combination of 3 effects: 1) reduced drain-side electric field, 2) reduced linear Vt reverse short channel effect, and 3) reduced SOI floating-body effects coming from lower drain-side impact ionization and increased body-source diode current. A further benefit of the reduced drain-side electric field is that asymmetric transistors show a substantial improvement of the HCI lifetime, as shown in Fig. 5.

Adding a source-side tilted extension implant results in a higher gate-source overlap, with an associated lower source-side series resistance and thus higher effective Vgs (1). This further increases drive currents, as shown in Fig. 6, to NIDSAT = 1290 µA/µm and PIDSAT = 820 µA/µm at 1.0 V, IOFF = 100 nA/µm. AC self- heating corrected, the values correspond to 1354 µA/µm NMOS and 857 µA/µm PMOS. These high drive currents are achieved at 1.2 nm EOT by fabricating the AFETs on industry-leading 5-way stressor integration on SOI, with embedded-SiGe, compressive and tensile overlayers, and 2 stress memorization techniques (4, 5).

At the same time that source-side tilted-extension increases gate-source overlap, it decreases gate-drain overlap, as shown in Fig. 7. Although the total overlap capacitance is unchanged compared to a standard symmetric transistor, this is an overall AC win due to the Miller effect on Cgd.

Optimization and AC Performance

When not properly optimized, however, asymmetric halo/ extension benefits can come at a cost of increased resistance on the drain side. This reduces the effective Vds, which, while it does not impact IDSAT, substantially impacts IDLIN, as shown in Fig. 8. Through implant optimization, however, IDLIN can be recovered, as shown in Fig. 9.

When the optimized asymmetric transistors are implemented into a ring oscillator (inverter with fanout = 3), there is a 12 % speed improvement at matched leakage, as shown in Fig. 10. This performance benefit is a combination of saturation drive current increase and

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improved Cgd Miller capacitance, at matched linear drive current.

Product Implementation

Product implementation can be a difficult process requiring the development of new design techniques to exploit asymmetric transistor features, design rules, which ensure compatibility between standard symmetric and asymmetric transistors, and integration optimization to minimize the additional masking and implantation costs. High requirements are placed on lithography processes to maintain mask blockage while avoiding mask shadowing. When properly implemented, however, the speed benefit can be substantial as shown in Fig. 11. Depending on the targeting and design, up to 12 % product-level performance improvement can be achieved at matched yield, as shown in Fig. 12. In addition, product reliability is expected to improve based on improved HCI characteristics.

Extendibility

The results described above have been achieved in AMD's 65nm and 45nm technologies, and demonstrate that the asymmetric transistors can scale well into the 32nm technology gate length regime. Fig. 13 shows the linear and saturated threshold voltage versus gate length rolloff comparing asymmetric and symmetric NMOS transistors. For the symmetric NMOS transistor, DIBL increases substantially as the gate length is scaled down. This is due to source-side and drain-side halos adding together increasing the linear threshold voltage.

The asymmetric transistor has the advantage that there is only a source-side halo, effectively suppressing this reverse short channel effect. However, there is an increase in saturated threshold voltage rolloff on the NMOS which would require tighter control of critical gate dimensions across the die. Fig. 14 shows that with the PFET transistor, the DIBL improvement does not come at the cost of saturated threshold voltage rolloff degradation. This demonstrates that there is a possibility of optimizing the rolloff versus DIBL relationship for NMOS as well.

At the larger gate pitches of 65nm technology, lithography techniques can be applied which allow an existing design to be adapted to include asymmetric transistors. This holds true for 45nm technology due to poly gate height scaling. However, given minimal poly gate height scaling going into 32nm, designs using asymmetric transistors will have to be done a priori due to lithography restrictions to avoid implant shadowing. This requires an extremely close collaboration between design and technology in order to clarify the distribution of active areas between symmetric and asymmetric transistors. With increased custom design effort, asymmetric transistors are extendable into future technology nodes.

Conclusion

Optimized asymmetric MOSFETs with significant performance and reliability improvement have been shown. Drive currents are improved 10-12 %, up to 1354 µA/µm NMOS and 857 µA/µm PMOS, while Cgd Miller capacitance is decreased. This leads to a 12 % ring oscillator improvement, and up to 12 % product-level improvement at matched yield. The developed technology and design techniques are highly manufacturable in the 65 nm and 45 nm technology nodes, and are scalable to future technologies.

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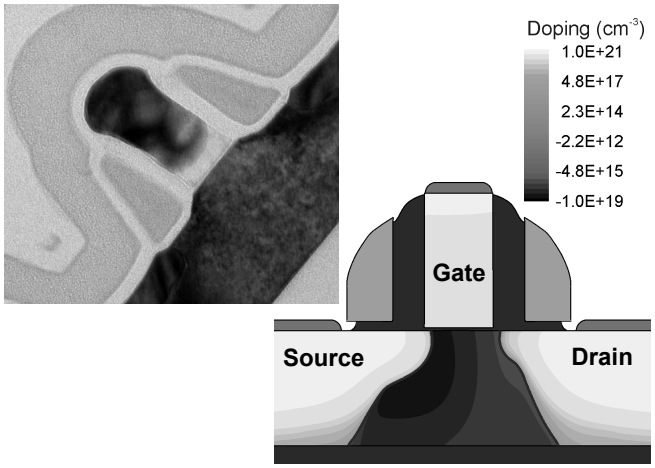

Fig. 1. 45 nm asymmetric NMOS device and simulated doping profile. The higher overlap and the steeper junction on the source side are caused by the tilted source-side halo and extension implantation.

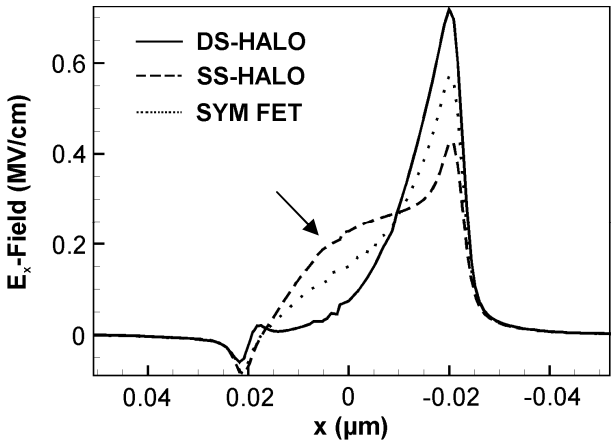

Fig. 2. Comparisons of the lateral electric field in the channel region. Source-side (SS) halos show a desirable high electric field near the source, low electric field near the drain. Drain-side (DS) halos have undesirable effects; a symmetric FET is a compromise.

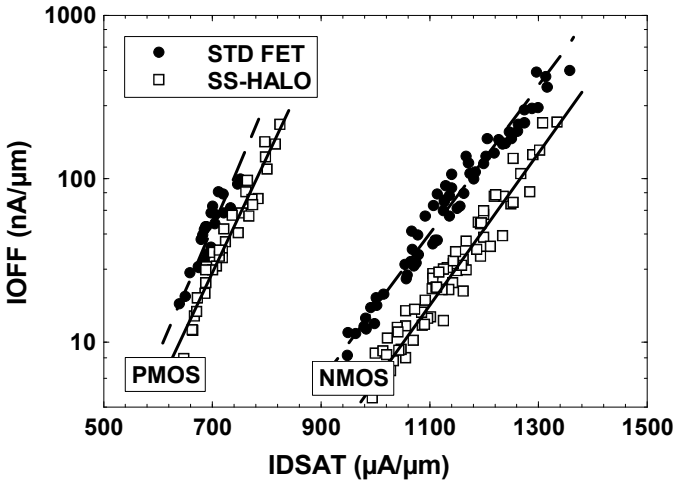

Fig. 3. NMOS and PMOS IOFF vs. IDSAT at 1.0 V showing SS-halo implantation improving NMOS and PMOS performance by 10 % and 8.5 %, respectively.

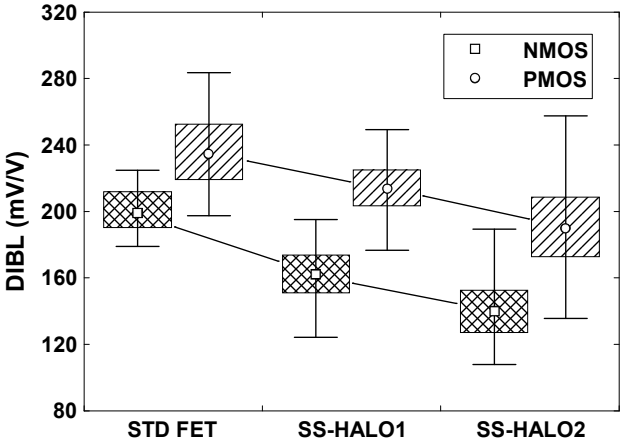

Fig. 4. DIBL behavior for different SS-halo tilt angles compared to a standard symmetric device.

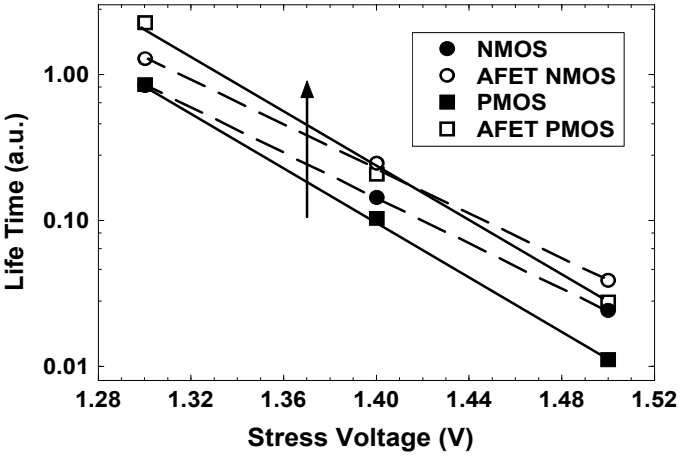

Fig. 5. Longtime reliability measurement shows an increase of HCI lifetime for AFETs which is related to the decrease in the electric field on the drain.

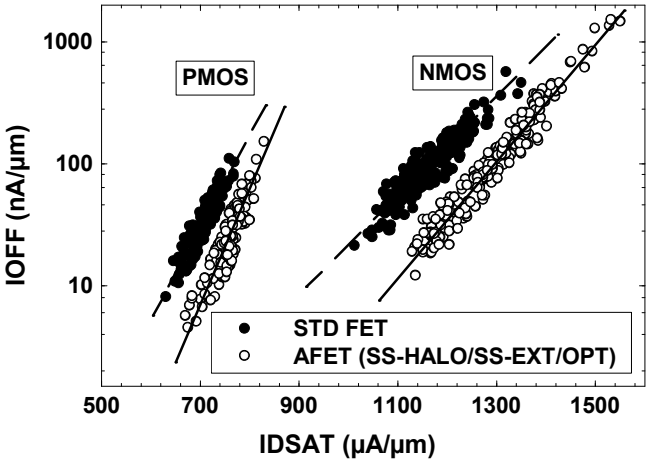

Fig. 6. NMOS and PMOS IOFF vs. IDSAT at 1.0 V showing optimized AFETs improving NFET and PFET by 12 % and 10 %, respectively.

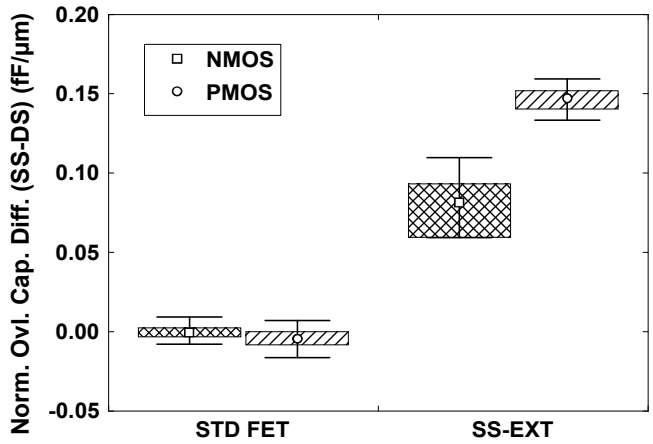

Fig. 7. Overlap capacitance difference of source-side to drain-side, at matched overall overlap capacitance. Drain-side overlap capacitance is 8 aF/µm lower for NMOS and 15 aF/µm lower for PMOS.

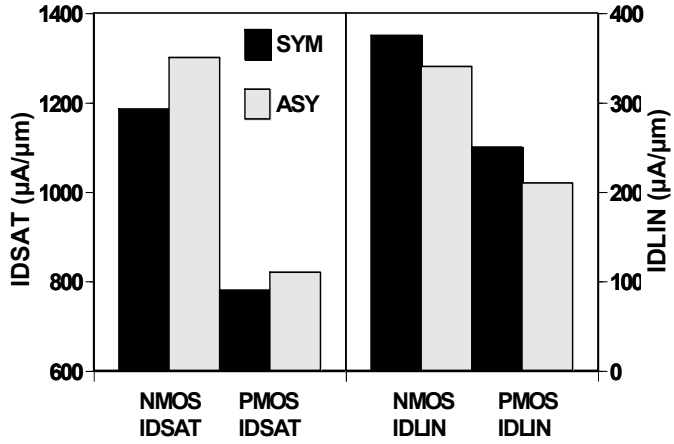

Fig. 8. IDSAT and IDLIN at IOFF = 100 nA comparison between symmetric and asymmetric halo/extension devices. The saturated drive current shows improvement, but linear drive current shows degradation on N- and PMOS devices.

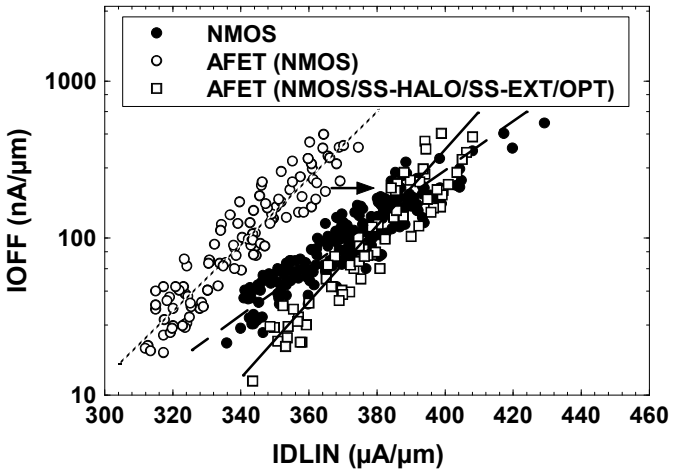

Fig. 9. NMOS linear drive current comparison of standard devices and AFETs. With implant optimization the 8 % IDLIN degradation is recovered.

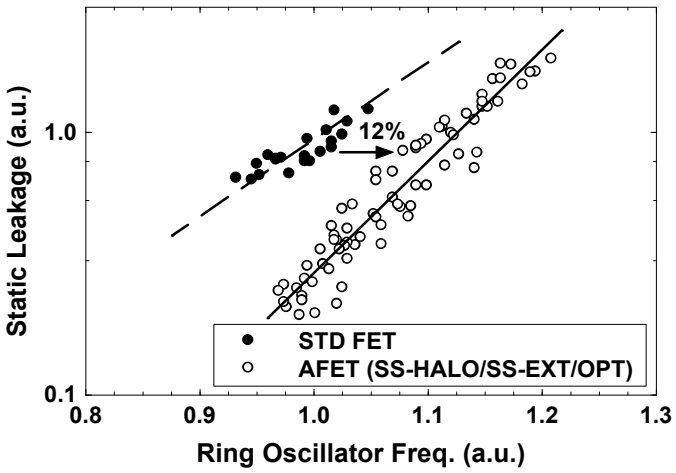

Fig. 10. Ring oscillator performance for standard and asymmetric devices. The optimized asymmetric devices show an increase in frequency of 12 %.

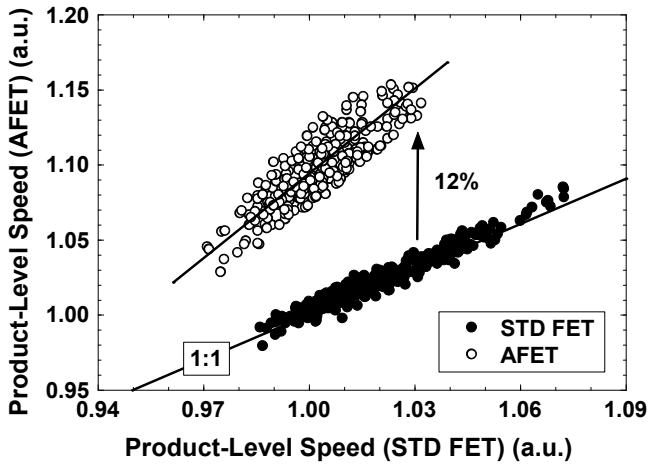

Fig. 11. Quad Core product level performance comparison between microprocessor parts where just standard or partially additional asymmetric devices where applied.

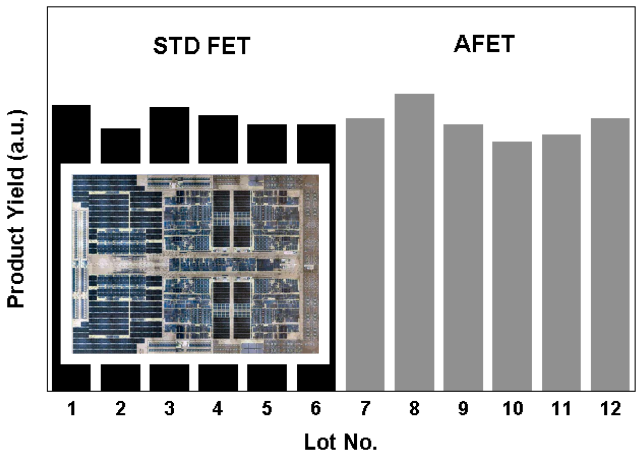

Fig. 12. Quad core microprocessor yield comparison between microprocessors where standard symmetric devices and AFETs were applied. (Inlet: 45 nm quad core µP)

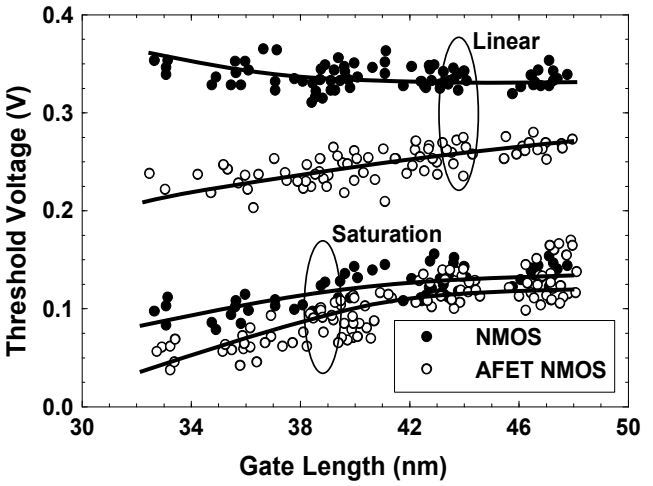

Fig. 13. NMOS threshold voltage (linear and saturation region) vs. gate length. Asymmetric NMOS shows a substantial decrease in DIBL at the cost of slightly increased saturated threshold voltage rolloff.

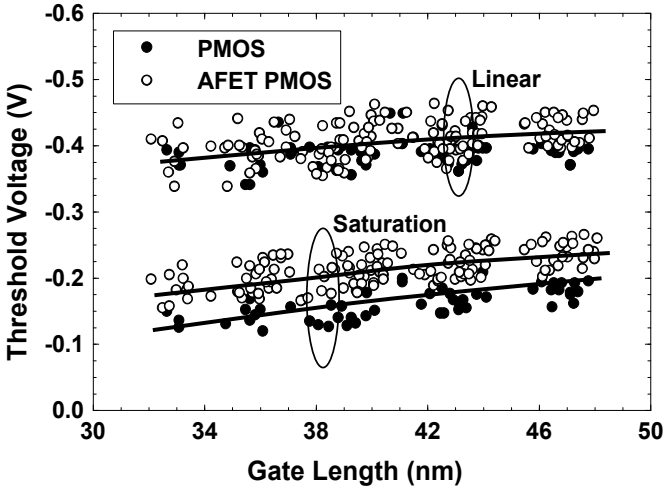

Fig. 14. PMOS threshold voltage (linear and saturation region) vs. gate length. Asymmetric PMOS shows a comparable threshold voltage rolloff to the symmetric doped devices.