EFFECT OF SOURCE/DRAIN EXTENSION DOPANT SPECIES ON DEVICE PERFORMANCE OF NON-DIFFUSIVE EMBEDDED SIGE STRAINED SOI P-MOSFETS

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ABSTRACT

This report shows the importance of source/drain extension dopant species on the performance of embedded silicon-germanium strained SOI p-MOSFET devices, in which the activation was done using only high temperature non-diffusive ultra fast annealing technologies. BF_2 and boron were investigated as source/drain extension dopant species. In contrast to unstrained silicon p-MOSFETs, boron source/drain extension implantations enhance device performance significantly compared to devices with BF_2 source/drain extension implantations. Measurements show a 30 % mobility enhancement and lower external resistance for the devices with boron source/drain extension implantations. The reason for this lies in the amorphization nature of BF_2 implantations. Remaining defects after implant annealing affect the stress transfer from the embedded silicon-germanium and the overall hole mobility which leads to the observed performance degradation. Furthermore, TCAD simulations reveal that the mobility degradation with BF_2 source/drain extension implantations is equivalent to almost 36 % strain relaxation of the embedded silicon-germanium.

INTRODUCTION

Ultra shallow junctions with sufficiently low resistance are necessary for continuous metal oxide semiconductor field effect transistor (MOSFET) scaling to the 32 nm technology node and beyond. In order to achieve these targets, it is indispensable to replace the conventional rapid thermal annealing (RTA) with high temperature non-diffusive ultra fast annealing (UFA) technologies like flash lamp annealing (FLA) (1) or non-melt laser spike annealing (LSA) (2). These new annealing technologies offer many advantages over conventional RTA techniques including high electrical activation, excellent lateral abruptness and limited dopant diffusion and the ability to engineer the extended defects resulting from the ion implantation.

Apart from aggressive junction scaling to support reduced gate lengths, there is a permanent need for improved performance and reduced power consumption. Recently, the main focus for improved transistor performance lies on mobility and drive current enhancement by the application of appropriate local stress. For advanced complementary MOS (CMOS) technologies, mobility enhancement techniques such as tensile strained overlayers and stress memorization techniques for the n-MOSFET and compressive strained overlayers and embedded silicon-germanium (eSiGe) for the p-MOSFET are standard features to improve device performance (3).

In an advanced CMOS process the new UFA techniques have been successfully implemented in addition to the conventional RTA to further improve state-of-the-art CMOS transistors. As a result, a transistor performance improvement could be achieved due to reduced poly depletion and reduced source-drain resistance. Furthermore, a full compatibility with eSiGe source-drain stressor and no deactivation with subsequent low temperature backend processing steps for the ultra fast annealing technologies in addition to a standard RTA could be demonstrated (4). One of the main integration challenge of the new UFA schemes as alternative to RTA is the implementation of the eSiGe in an advanced p-MOSFET device to maintain the advantages of this mobility enhancement technique. The new annealing technologies must be in a position to recover the implantation damage without any strain relaxation of the eSiGe stressor.

Boron is the first choice as a p-MOSFET dopant. This species can be introduced into silicon via monomer B^+ implantation or by using the molecular species BF_2^+. In addition, there exist alternative molecular p^+ dopant species such as $B_{10}H_{14}$ and $B_{18}H_{22}$ which offer high quality junctions with higher activation levels in comparison to boron or BF_2 (5). But, they are still under investigation and therefore not a content of this work. Usually, a pre-amorphization implantation (PAI) is used to eliminate dopant channeling. A PAI can lead to higher dopant activation, but the residual end-of-range (EOR) damage created by the amorphization implantation results in high damaged junctions when using these advanced dopant activation techniques with minimal thermal budget (6). Furthermore, the use of a PAI in conjunction with the eSiGe p-MOSFET stressor can lead to strain relaxation effects which have a negative impact on device performance.

For that reason, a comparative study of BF_2 and boron as source/drain extension (SDE) dopant species on the performance of eSiGe strained SOI p-MOSFET devices without PAI is presented, in which the activation annealing was done using only high temperature non-diffusive UFA technologies.

EXPERIMENTAL AND SIMULATION DETAILS

P-MOSFET devices with a physical gate length of 38 nm were fabricated on SOI wafers using SiON as gate dielectric and polysilicon as gate material in a 45 nm SOI technology with contacted poly pitch of 190 nm. To avoid poly depletion issues, the poly was doped before gate patterning and a gate annealing was added. Before SDE definition, the eSiGe mobility enhancement technique for the p-MOSFET with a germanium content of 22 % ($Si_{0.78}Ge_{0.22}$) was implemented. Subsequent to halo and extension implants, an offset spacer was formed followed by deep source/drain implantations. To activate the dopants in the SDE and deep source-drain area, exclusively UFA was carried out before silicidation. Figure 1 shows a TEM cross-section of a diffusionless 38 nm SOI p-MOSFET with the eSiGe stress technique after contact formation.

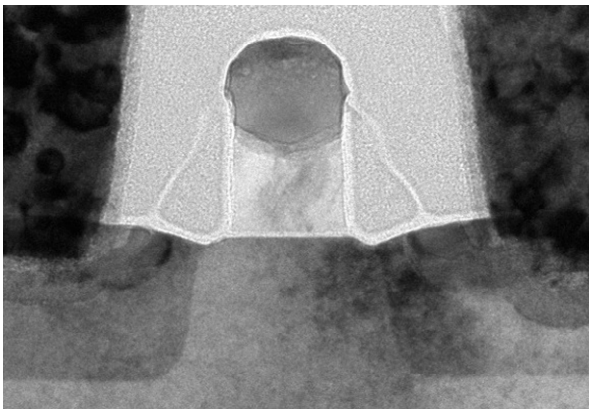

Figure 1: TEM cross section of a diffusionless 38 nm SOI p-MOSFET with the eSiGe stress technique.

The halo implant parameters (energy, dose, tilt) are identical to keep the channel doping profile unchanged for the investigated devices (B-SDE, BF_2-SDE). The energies of the SDE implants were chosen so that the peak of the boron profile occurred at the same depth for both implants. The implant conditions of the B-SDE are 0.5 keV with a dose of $1x10^{15}$ cm^{-2} whereas the implant parameters of the BF_2-SDE are 2.3 keV with a marginal higher implant dose. Thus, the transistors are targeted for identical threshold voltage and metallurgical gate length for a fair comparison. The latter is deviated from the overlap capacitance. Furthermore, a set of p-MOSFETs with and without eSiGe was processed.

In addition, process and device simulations using SYNOPSYS Sentaurus TCAD software have been performed to clarify the observed experimental behavior. The channel stress was calculated using 2D process simulation where all intentional and unintentional stress sources and stress evolution during the entire process flow are taken into account. To simulate the phenomenon of diffusionless doping activation, a model was used that can simulate the inhomogeneous thermal distribution, which results in better accuracy for stress calculation as well as heat transfer delay to the region in which the devices form. Furthermore, germanium chemical and stress effects on dopant diffusion and activation were also taken into account. The device simulation uses various physical models. In the basic approach, carrier mobility is simulated using the hydrodynamic transport model. The simulations also include band-to-band tunneling and a hole mobility model that accounts for the valence band splitting and intervalley redistribution of holes due to mechanical stress. The simulation models were calibrated using measured SIMS profiles, TEM cross sections, transfer and output characteristics as well as other electrical data on the fabricated transistors listed above.

RESULTS AND DISCUSSION

Figure 2 represents the I_{on}/I_{off} performance characteristics for p-MOSFET devices with and without eSiGe in the saturation and linear regime. In contrast to unstrained silicon p-MOSFETs B-SDE implantations enhances device performance significantly compared to devices with BF_2-SDE implantations. A 10 % saturation as well as a 16 % linear drain current improvement at $I_{D,off}$ = 100 nA/µm can be observed for eSiGe strained p-MOSFET devices with B-SDE implantations in comparison to eSiGe strained p-MOSFET devices with BF_2-SDE implantations.

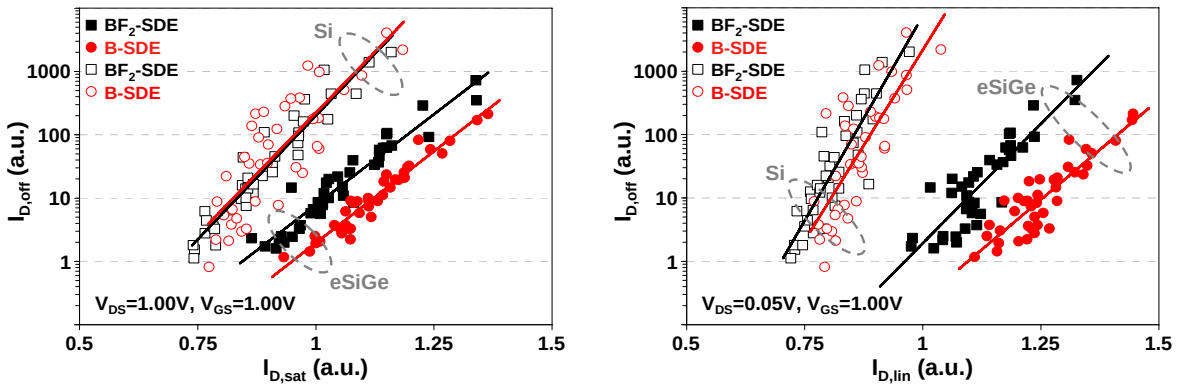

Figure 2: $I_{D,on}/I_{D,off}$ characteristics of p-MOSFET devices with different SDE implantations with (eSiGe) and without (Si) eSiGe (left: saturation drain current $I_{D,sat}$; right: linear drain current $I_{D,lin}$).

In order to investigate the possible origin of the performance improvement with B-SDE implantations, several parameters were monitored. An extraction of effective hole mobility was performed to evaluate the influence of the two different SDE implantations on the carrier mobility based on the $\Delta R_{Total}/\Delta L_G$ method (7). Note that, by employing this approach, the mobility can be extracted while eliminating the series resistance effects.

Figure 3 plots the total resistance R_{Total} as a function of gate length L_G at constant overdrive for eSiGe strained and unstrained devices with B- and BF_2-SDE implantations. A linear curve fitting (lines in Figure 3) of R_{Total} vs. L_G was used to determine the carrier mobility as well as the parasitic resistance (intersection with y-axis). Differences in the slope of the curves indicate different carrier mobilities.

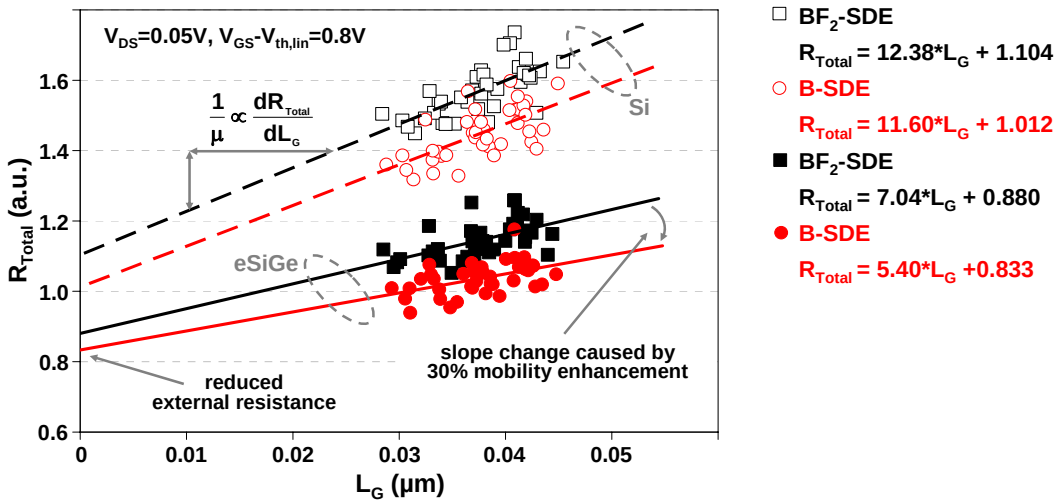

Figure 3: Total resistance R_{Total} as a function of gate length L_G at constant overdrive showing a 30 % hole mobility improvement with B-SDE compared to BF_2-SDE.

Three major facts are obvious:

1. The parasitic resistance (intersection with y-axis) is increased with BF_2-SDE implantation for eSiGe strained as well as for unstrained devices.

2. There are only marginal mobility differences between devices with B- and BF_2-SDE in the case of p-MOSFETs without eSiGe. The curves have only an offset which is determined by the different parasitic resistance.

3. In the case of p-MOSFETs with eSiGe, devices with B-SDE implantations demonstrate a reduced $\Delta R_{Total}/\Delta L_G$ slope in comparison to devices with BF_2-SDE implantations indicating a mobility enhancement which is in the range of 30 %.

$$\frac{\mu_{B-SDE}}{\mu_{BF_2-SDE}} \propto \frac{7.04}{5.40} = +30\%$$

The reason in the former case can be explained by the impact of the fluorine on boron activation. With the BF_2 implant the sheet resistance is generally higher than with the boron implant. This is due to the fact that the fluorine is overlying the boron profile which is known to decrease activation (8-10). The cause in the latter case lies in the amorphization nature of BF_2-SDE implantations as shown in Figure 4. In contrast to B-SDE implantations, BF_2-SDE implantations create an amorphous layer.

One explanation for the mobility degradation can be that the subsequent annealing to activate the dopants and regrow the amorphous layer decrease the strain energy in the structure and cause them to relax by forming misfit and threading dislocations which leads to a reduction in strain (11).

Another reason for the reduced mobility could be residual EOR defects created by the BF_2-SDE implantation which also influence the stress transfer from the eSiGe to the channel. It is important to note that UFA, despite the very high temperature, does not fully dissolve the defects in the silicon respectively silicon-germanium crystal, probably due to the very short time scale of the annealing (12).

As a result one can assume that the Si/SiGe interface will not fully be recovered with the UFA and the remaining defects affect the stress transfer from the eSiGe and the overall hole mobility which leads to the observed performance degradation with BF_2-SDE in combination with the eSiGe stressor.

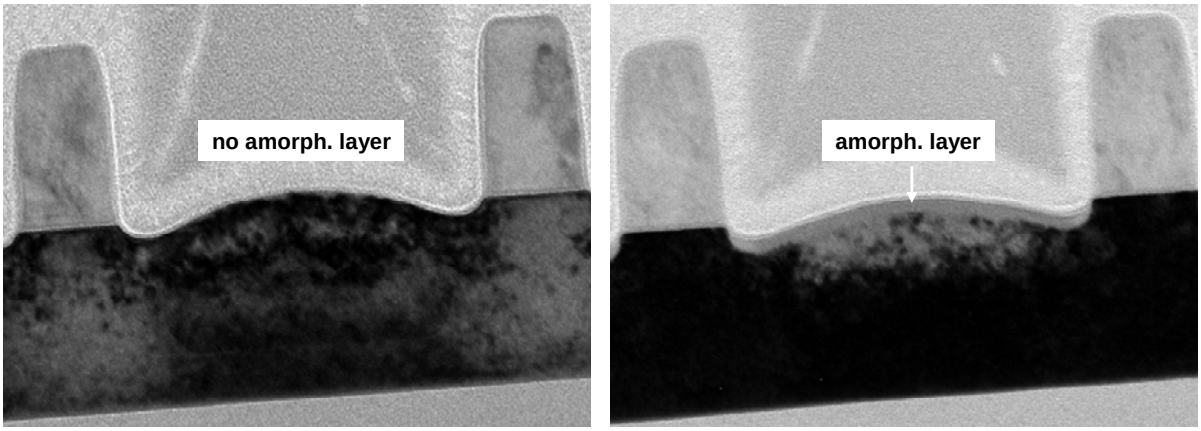

Figure 4: TEM cross sections after halo and SDE implantation for devices with B-SDE (left) and BF_2-SDE (right). In contrast to B-SDE implantations, the BF_2-SDE implantations create an amorphous layer which leads to residual EOR defects after millisecond annealing.

An argument for the presence of defects shows Figure 5. Here, the impact of both SDE implantations of the diode junction leakage for eSiGe strained p-MOSFETs in the reverse and forward direction is presented. With the use of BF_2-SDE implantation a considerable increase in junction leakage for both directions is noticeable. Since the channel-, body- and SD-doping are fixed and the SDE doping profile are almost the same of the investigated devices, the higher junction leakage with BF_2-SDE can only be caused by higher number of defects in the p/n-junction which leads to an increased generation-recombination current.

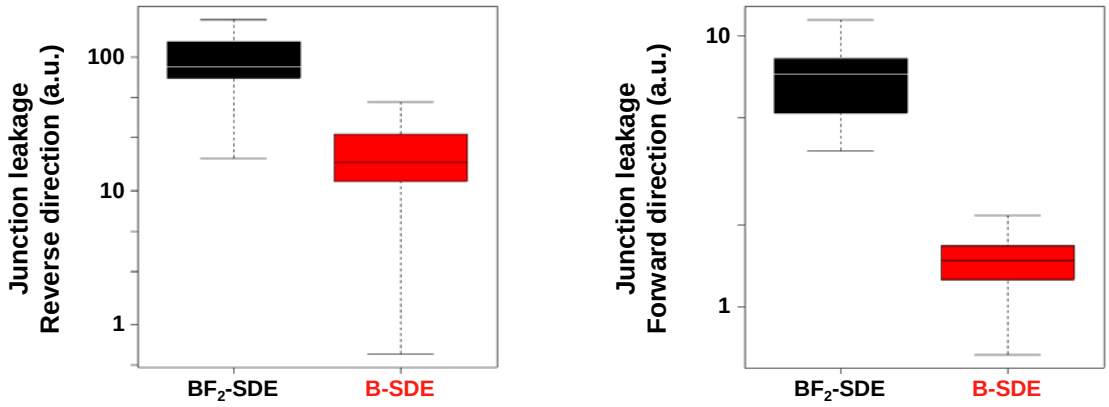

Figure 5: Junction leakage in reverse (left) and forward (right) direction of eSiGe strained p-MOSFET devices with different SDE implantations.

To clarify the observed experimental behaviour, TCAD simulations have been carried out. After calibration of the experiments for B-SDE implantation in Si (germanium content of 0 %) and eSiGe (germanium content of 22 %), a set of simulations of p-MOSFET devices with different germanium contents were performed. Figure 6 shows the simulated total resistance R_{Total} as a function of gate length L_G for varying germanium content of the eSiGe. As expected, due to higher overall hole mobility in the channel and in the eSiGe with increased germanium content, a continuous decrease in the $\Delta R_{Total}/\Delta L_G$ slope as well as a reduced total resistance is recognizable. A comparison of the different simulated $\Delta R_{Total}/\Delta L_G$ slopes with the BF_2-SDE implantations in eSiGe reveal that a simulated B-SDE implantation into eSiGe with a germanium content of 14 % fits well with the experimental data for BF_2-SDE implantation into eSiGe with a germanium content of 22 % (Figure 7). This means that the mobility degradation with BF_2-SDE implantations is equivalent to almost 36 % strain relaxation of the eSiGe.

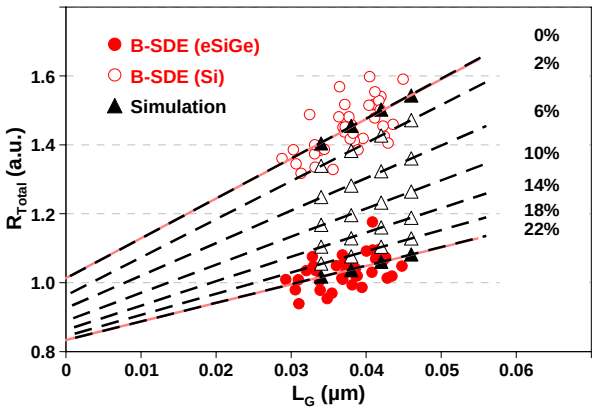

Figure 6: Simulated total resistance R_{Total} as a function of gate length L_G for varying germanium content of the eSiGe (triangle). Experimental data are shown for comparison (circles).

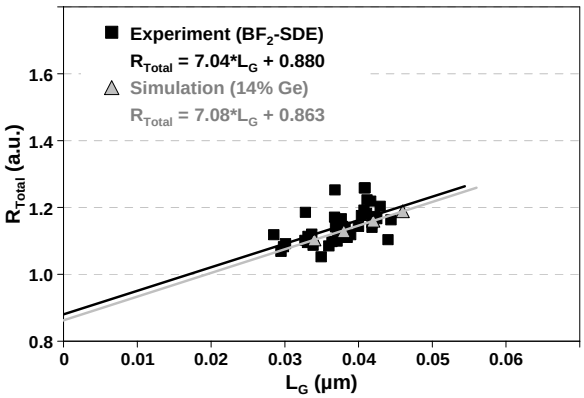

Figure 7: The simulated B-SDE implantation into eSiGe with a germanium content of 14 % (triangle) fits well the experimental BF_2-SDE implantation into eSiGe with a germanium content of 22 % (rectangle).

CONCLUSION

BF_2 and boron as source/drain extension dopant species on the performance of eSiGe strained SOI p-MOSFET devices without PAI were investigated. The results of the experiments show that self amorphization implantations which create a huge amount of end-of-range defects have a negative impact on performance of embedded silicon-germanium strained p-channel transistors in which the activation annealing was done using only high temperature diffusionless annealing technologies like flash lamp annealing or non-melt laser spike annealing. Simulations have proven that the mobility degradation with BF_2 source/drain extension implantations is equivalent to almost 36 % strain relaxation of the embedded silicon-germanium. These results show that low damage creating source/drain extension implantations in combination with embedded silicon-germanium are necessary to enhance the performance of diffusionless strained SOI p-MOSFETs.

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