DETAILED SIMULATION STUDY OF EMBEDDED SIGE AND SI:C S/D STRESSORS IN NANO SCALED SOI MOSFETS

S. Flachowsky, R. Illgen, T. Herrmann, W. Klix, and R. Stenzel
Department of Electrical Engineering, University of Applied Sciences Dresden, Friedrich-List-Platz 1, D-01069 Dresden, Germany

I. Ostermay
Fraunhofer Center für Nanoelektronische Technologien, Königsbrücker Straße 180, D-01099 Dresden, Germany

A. Wei, J. Höntschel, M. Horstmann
AMD Fab 36 LLC & Co. KG,
Wilschdorfer Landstrasse 101, D-01109 Dresden, Germany

ABSTRACT

Strained silicon techniques have become an indispensable technology feature, enabling the momentum of semiconductor scaling. Embedded silicon-germanium (eSiGe) is already widely adopted in the industry and delivers outstanding p-MOSFET performance improvements. The counterpart for n-MOSFET is embedded silicon-carbon (eSi:C). However, n-MOSFET performance improvement is much more difficult to achieve with eSi:C due to the challenging process integration. In this study, detailed TCAD simulations are employed to compare the efficiency of eSiGe and eSi:C stressors and estimate their potential for performance enhancements in future nano scaled devices with gate lengths down to 20 nm. It is found, that eSiGe as a stressor is superior to eSi:C in deeply scaled and highly strained devices due to an easier process integration, reduced parasitic resistance and non-linear effects in the silicon band structure favouring hole mobility enhancement at high strain levels.

INTRODUCTION

Traditional complementary metal oxide semiconductor (CMOS) scaling has offered advantages in both device performance and density, driving higher system performance at lower cost and higher yield. However, with further scaling, the conventional MOSFET architecture is reaching its fundamental limit, requiring thin gate oxides and high channel doping that lead to high leakage and low device performance. Technological innovations are proposed to maintain the continual improvement trajectory laid out in the ITRS roadmap. One of this is mobility and drive current enhancement by the application of appropriate local stress. Current leading-edge CMOS technologies feature multiple process-induced stressors such as compressive and tensile overlayers, embedded SiGe, and stress memorization techniques (1),(2). Other strain techniques like biaxial tensile strained substrates (3), embedded silicon-carbon layers (4), and strained metal gates and contact fill materials (5) are considered as potential performance boosters for next technology generations.

Especially the embedded source/drain (S/D) stressors, i.e. embedded $Si_{1-x}Ge_x$ (eSiGe) and embedded $Si_{1-y}C_y$ (eSi:C), have attracted much attention. Starting with the 90 nm technology, eSiGe is now widely adopted in volume manufacturing and has proven doubtlessly as a very effective stressor in p-MOSFET devices. Apart the generation of high compressive channel stresses, eSiGe also contributes to a reduced parasitic S/D resistance, due to beneficial band alignments in the SiGe alloy resulting in reduced contact

resistance. On the other hand, integrating epitaxial eSi:C into n-MOSFET source/drain areas was found extremely difficult, and only limited progress in high-performance transistors was reported across the semiconductor industry despite the enormous effort spent on this subject. This can be ascribed to the demanding requirements in process integration. Although carbon is a much smaller atom than silicon, and thus it requires only a relatively small amount of carbon (1-2 at%) to create a useful level of strain, the challenge lies in the very low solid solubility of carbon in silicon which is < 0.7 ppm (6). Metastable epitaxial deposition processes such as ultra high vacuum CVD, low-pressure CVD with high-order silanes, solid phase epitaxial regrowth with millisecond annealing are required to create highly strained Si:C films. To place the carbon on substitutional lattice sites is one issue; another is to keep it there throughout the device fabrication using low-thermal budget processes and avoid damaging implantation steps. Otherwise carbon precipitates into carbide cluster which not only relaxes the strain but also degrade the electrical properties of the film.

Unaffected from these practical limitations, 2-D process and device simulations are employed to study and compare the potential of both strain techniques, eSiGe and eSi:C, for performance enhancement in future technology nodes. Former simulation work about eSiGe (7),(8) or eSi:C (9) is mostly limited to mechanical stress calculations. It was found, that in terms of stress generation, the eSiGe technique is very similar to eSi:C (10). However, the different impact of strain on electrical device parameters such as mobility and drive current was not studied. Since strain and mobility are not linearly correlated, at least for the high strain region, detailed investigations on potential performance benefits are needed to evaluate the efficiency of these strain techniques in future nano scaled devices.

STRAINED SILICON PHYSICS

Fundamentally, application of mechanical stress on a crystal changes the interatomic spacing. Associated modifications in the electronic band structure and density of states contribute to changes in carrier mobility ($\mu = e\tau/m^*$) through modulated effective transport masses (m^*) and modified scattering rates ($1/\tau$). The strain effects on mobility are anisotropic and carrier effects are different for electrons and holes. For example, tensile strain (as induced by eSi:C) along the carrier transport direction enhances the electron mobility whereas it degrades hole mobility, which in turn can be enhanced with compressive strain using eSiGe. Many other material properties are also altered by strain fields including band gap, diffusion of dopants, and oxidation rates (11).

For electrons under uniaxial tensile strain, the six-fold degenerated conduction band valleys are split into two groups. The two-fold valleys ($\Delta 2$) are lowered in energy compared to the four-fold valleys ($\Delta 4$) which leads to increased electron occupancy in the $\Delta 2$ valleys. This yields two beneficial effects for mobility: Increasing fractional population of $\Delta 2$ valleys with a lower effective transport mass and less phonon scattering between $\Delta 2$ and $\Delta 4$ valleys. Beside this, another effect arises for uniaxial strain along the <110> direction, which is the common channel direction in current CMOS technologies. The off-axis deformation of the crystal structure leads to shear strain components and corresponding deformation of the band structure which cause a change in the effective mass of electrons in the $\Delta 2$ valleys (12). Compared to electrons, the physics that governs hole transport is less intuitive. Because the relaxed silicon valence band consists of degenerate valleys with a high degree of band warping, hole transport in silicon is particular sensitive to strain. In general, strain splits the degenerate valley extrema of light and heavy hole bands and modulates the band curvature and, therefore, the valley occupancy, effective mass, and scattering rates (11).

EXPERIMENTAL AND SIMULATION DETAILS

PROCESS SIMULATION

Using SYNOPSYS Sentaurus TCAD software, 2-D finite element simulations are performed to create various structures and analyze the strain distribution therein. Starting with silicon on insulator substrate (SOI, 74 nm silicon film on 145 nm buried oxide layer) the gate stack is structured with L_G = 40 nm physical gate length featuring 1.35 nm SiON gate oxide and polysilicon as gate material. That follows a disposable spacer formation to adjust the proximity P of the future embedded S/D stressor to the channel (Figure 1) which is 15 nm by default. A 50 nm deep recess is etched in the S/D regions of the transistor and refilled epitaxially with $Si_{0.77}Ge_{0.23}$ or $Si_{0.971}C_{0.029}$ to the original silicon level. Due to the lattice mismatch with the underlying silicon substrate 1 % compressive / tensile in-plane strain arises within the epitaxial film. The process continues with the disposable spacer removal, junction and silicide formation and finishes with contact formation. The transistor channel lies in a <110> direction on a (001) wafer.

The mechanical parameters (elastic modulus E, Poisson ratio v, etc.) of SiGe are obtained by those of silicon and germanium by linear interpolation, dependent on alloy composition. For Si:C the elastic constants are taken equal to silicon, an approximation that is valid for small concentrations of carbon (13). The simulator uses the plane-strain condition, in which the out-of-plane elongation is set to zero, which is a valid assumption for large width transistors studied in this work. Silicon, SiGe and Si:C are treated as anisotropic elastic materials and it is assumed that carbon in Si:C resides fully substitutional on lattice sites to create maximum strain. Strain was extracted as average in the channel in 2 nm depth below the surface. The perpendicular and shear strain components are not considered, since they were found to be much smaller than the lateral or vertical strain components.

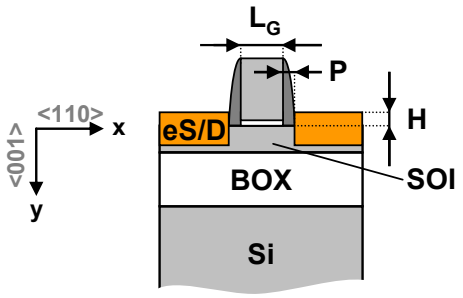

Figure 1: Schematic layout of strained transistor with embedded S/D (eS/D) stressor.

L_G – gate length
P – stressor-to-channel proximity
H – fill height over the original silicon level

DEVICE SIMULATION

The energy-balance and quantum-mechanical models were used in the device simulations. The effects of ionized impurity scattering were accounted for via a concentration dependent mobility model. A model which accounts for effects of the lateral field dependence on mobility was employed and a perpendicular field dependence model was used to model the effects of the Si/SiO_2 interface. The strain-dependent electron mobility was calculated based on the valley-occupancy model (14) including the effective mass variation under shear strain (15), while the strain-dependent hole mobility is based on the ellipsoidal valence band modulation (16). The strain-induced band gap narrowing was taken into account based on the deformation potential theory. More details of the above mentioned models can be found in (17).

MODEL CALIBRATION

For calibration purpose strained p-MOSFET devices with eSiGe were processed using the CMOS flow described in (1). Other intentional stress sources like compressive overlayers were omitted to clearly separate the strain effect of the eSiGe. Process and device model parameter were calibrated using measured secondary ion mass spectrometry (SIMS) profiles, transmission electron microscopy (TEM) cross sections and measured electrical device characteristics. For n-MOSFETs no experimental data was available for the calibration of the eSi:C stressor which instead was done using unstrained and strained devices by means of tensile overlayer films.

RESULTS AND DISCUSSION

EMBEDDED SILICON-GERMANIUM

Figure 2 shows the lateral and vertical strain components in a p-MOSFET with SiGe in the S/D regions. If the $Si_{0.77}Ge_{0.23}$ is fully strained to match the lattice constant of the underlying substrate the resulting lateral strain would be -1.0 %, i.e. the SiGe is laterally compressed. However, as can be seen in Figure 2, the SiGe region is partially relaxed rather than fully compressed. This is because the silicon region immediately beneath the SiGe stressor partially complies with the larger lattice constant of SiGe resulting in a tensile ε_{xx}. Partial relaxation of SiGe increases towards the top surface. The eSiGe stressor compresses the silicon channel region laterally, leading to large compressive strain ε_{xx} that extends throughout the channel region and becomes largest near the surface where carrier transport takes place.

Near the vertical heterojunction, the SiGe lattice attempts to stretch the silicon lattice vertically (i.e. tensile strained). The vertical strain in the silicon region decays fairly rapidly towards the middle of the channel. Both, the lateral compressive strain and the vertical tensile strain in the channel region contribute significantly to hole mobility enhancement and thus to drive current improvement in p-MOSFET devices.

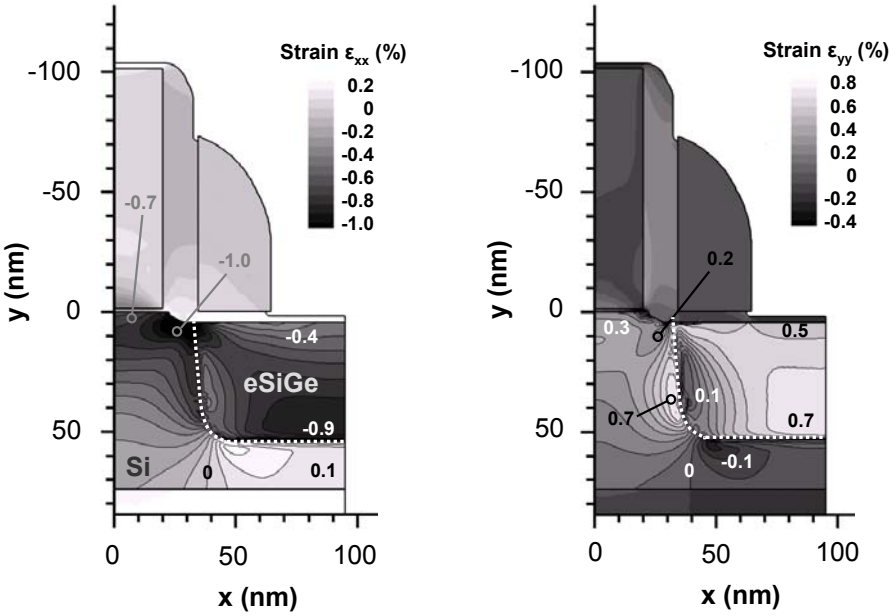

Figure 2: Lateral ε_{xx} and vertical ε_{yy} strain distribution in p-MOSFET with eSiGe in the S/D regions.

The induced strain fields depend on various material and geometrical device parameters, e.g. gate length, SiGe proximity to the channel, SiGe depth, and alloy composition. A reduction of the SiGe proximity to the channel does increase the channel strain significantly due to the closer source and drain side stressor, Figure 3.

The compressive strain and the presence of germanium in silicon affect the band gap and point-defect equilibrium concentration such that the boron diffusion is retarded. This becomes noticeable in the unexpected behavior of the drive current degradation for closer SiGe proximities of devices with identical implantation conditions (implant-matched) although the channel strain increases as expected. With closer proximities the highly doped extension regions diffuse less under the gate, resulting in higher metallurgical gate lengths, higher threshold voltage and reduced drive current (Figure 4).

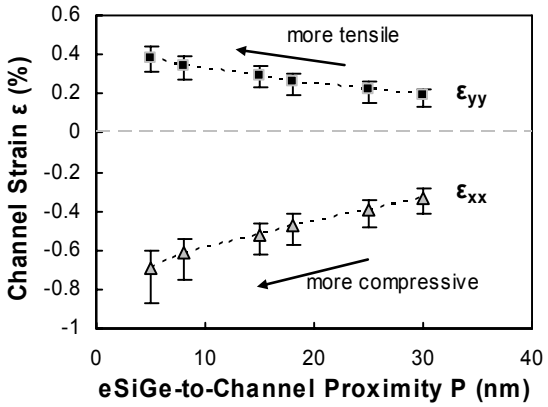

Figure 3: Lateral ε_{xx} and vertical ε_{yy} channel strain in p-MOSFET with eSiGe for different proximities to the channel. The symbols plot the average of each strain component in the channel region 2 nm below the Si/SiO_2 interface. The bars indicate the maximum and minimum strain magnitudes along this cut-line.

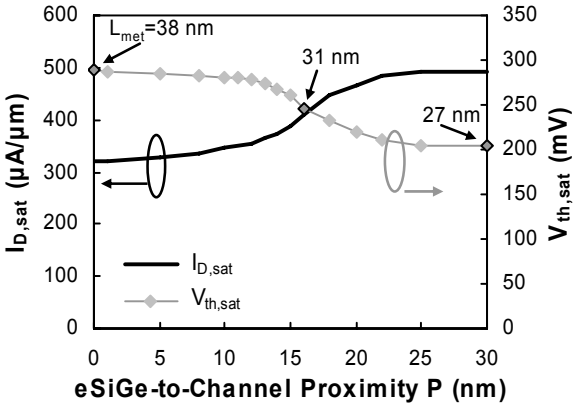

Figure 4: Drive current $I_{D,sat}$ and threshold voltage $V_{th,sat}$ of implant-matched p-MOSFET with eSiGe for different proximities to the channel. The metallurgical gate length (distance from source-side pn-junction to the drain-side pn-junction) is indicated for specific proximities.

In order to compensate for the retarded boron diffusion, the S/D extension dose was increased accordingly to match the metallurgical gate length and thus the threshold voltage for all proximities. The corresponding drive current enhancement for these threshold-matched devices is shown in Figure 5. Experimental data is plotted for comparison and confirms the well calibrated model parameters.

The impact of the eSiGe fill height on the drive current enhancement is shown in Figure 6. An overfill correlates with a higher SiGe volume, resulting in higher strain fields and thus higher drive current. This is again in excellent agreement with experimental data.

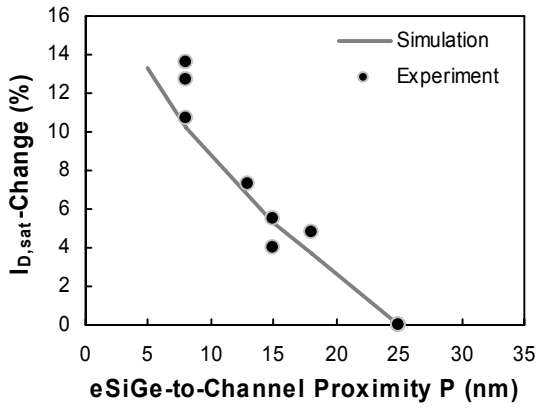

Figure 5: Relative drive current enhancement for closer eSiGe-to-channel proximities for both, experiment and simulation of p-MOSFET devices with matched threshold voltage.

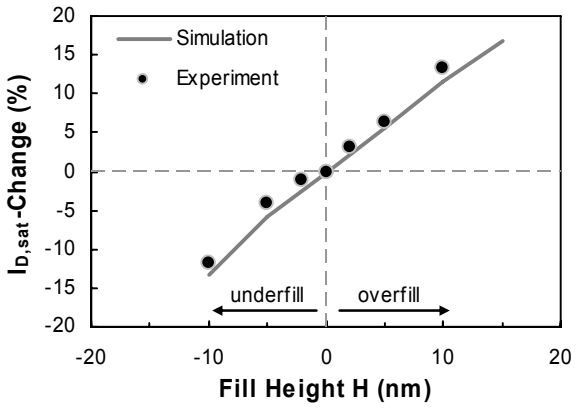

Figure 6: Relative drive current enhancement for varying eSiGe fill heights for both, experiment and simulation.

EMBEDDED SILICON-CARBON

The strain response of an n-MOSFET with eSi:C to layout variations is very similar to that described before for p-MOSFET with eSiGe, despite that the strain components are complementary, which in turn is required for n-MOSFET performance enhancement. The alloy composition is another design parameter affecting transistor performance. Higher carbon mole fractions yield in higher strained Si:C-layers and higher drive current enhancements, as shown in Figure 7. However, despite a doubling of the particular carbon fraction relative to the next smaller one, there is not a doubling in drive current enhancement. The drive current enhancement per % C is higher for low carbon fractions than for higher fractions. This "saturation" effect is characteristically for n-MOSFETs and is explained in more detail in the next section.

The silicon recess, caused by reactive ion etching during gate sidewall spacer formation, not only modifies the surface, it also alters the strain transfer from the embedded stressor into the channel. It is found that a reduction of the silicon recess or even an elimination improve device performance due to an improved mechanical coupling between the stressor and the channel. The strain in the channel increases from 0.7 % to 0.9 % (Figure 8) resulting in additional 5 % drive current enhancement. This effect can analogous be observed in eSiGe strained p-MOSFETs.

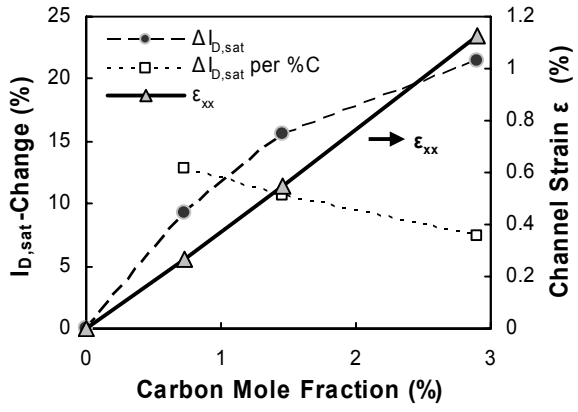

Figure 7: Simulated drive current enhancement and lateral channel strain for different carbon mole fractions in the Si:C layer.

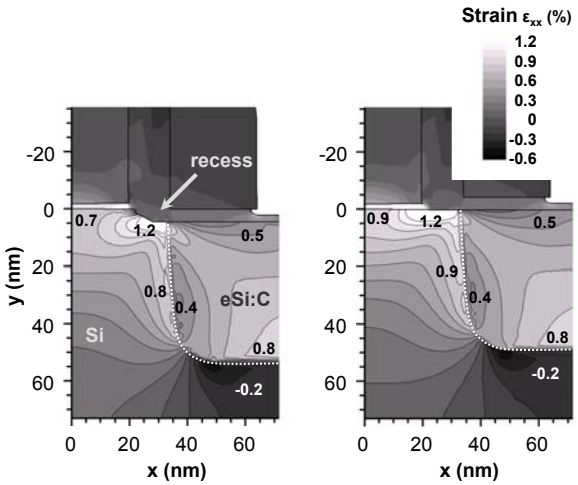

Figure 8: Lateral strain ε_{xx} distribution in n-MOSFET with embedded Si:C with (left) and without (right) silicon recess.

COMPARISON OF EMBEDDED SILICON-GERMANIUM AND SILICON-CARBON

For identical (but complementary) strain fields in the transistor channel, the eSiGe S/D stressor is significantly more effective than the eSi:C S/D stressor, as pointed out in Figure 9 and Figure 10 for increasing strain levels modulated either by stressor-to-channel proximity or the stressor volume. Drive current enhancement in p-MOSFET increases continuously with increasing strain and even exhibits a slightly super linear behavior in the very high strain region, as also indicated by the experimental data in Figure 5. Contrary, the drive current enhancement in n-MOSFET with eSi:C saturates for higher strain and no further improvement is possible when reducing the proximity below 10 nm or increasing the Si:C fill height beyond 10 nm over the original silicon level. Taking into account the effective mass change under <110> strain, higher improvements are achievable, but the saturation is still existent.

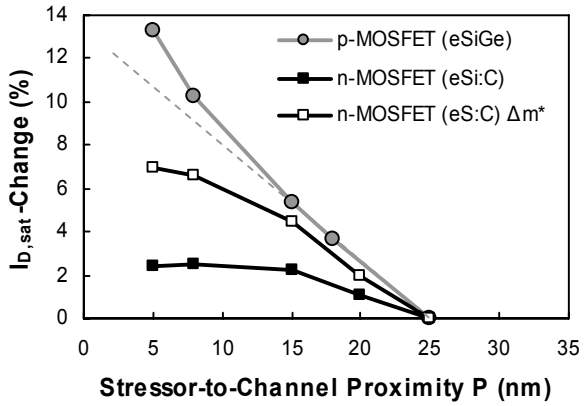

Figure 9: Relative drive current enhancements in dependence of the stressor-to-channel proximity for n-MOSFET with eSi:C and p-MOSFET with eSiGe.

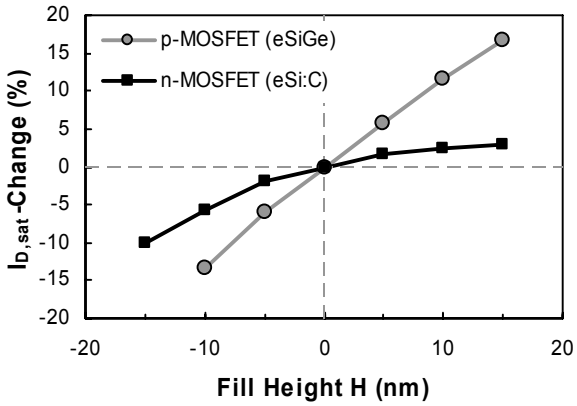

Figure 10: Relative drive current enhancements in dependence of stressor volume for n-MOSFET with eSi:C and p-MOSFET with eSiGe.

The origin for these differences lies in the strain-mobility-relation for electrons and holes. For small strain levels (-0.1 % < ε < 0.1 %) the change in the mobility is linear to changes in strain. This corresponds to the classical piezoresistance effect (18). However, for the high strain regions deviations from this relationship appear. An increase in electron mobility arises from transfer of electrons into the lower-energy minima Δ2 along the <001> axis with the lower conductivity mass in conjunction with an intervalley scattering suppression. At ε~0.8 %, there is sufficient conduction-band splitting to completely repopulate carriers from Δ4 into Δ2 valleys and simultaneously suppress intervalley phonon scattering, and little improvement in electron mobility takes place for further increase in strain (19) as it is shown in Figure 11. The impact of the effective mass reduction of Δ2 electrons under <110> uniaxial tensile strain is also illustrated. Although in this case the saturation in electron mobility enhancement is not that pronounced, the absolute improvements are still significant lower than for holes at the same strain level. The hole mobility enhancement at small strains can be considered to be solely from hole redistribution among the split bands and consequently the conductivity mass change. In the large strain case (ε < -0.6 %), the hole mobility enhancement is determined by both the conductivity mass and phonon scattering rate reduction. As the splitting is larger than the optical phonon energy (20) intervalley scattering is totally suppressed and scattering takes place only within the top band (21). That is the reason for an increased improvement rate at higher compressive strain levels (Figure 12).

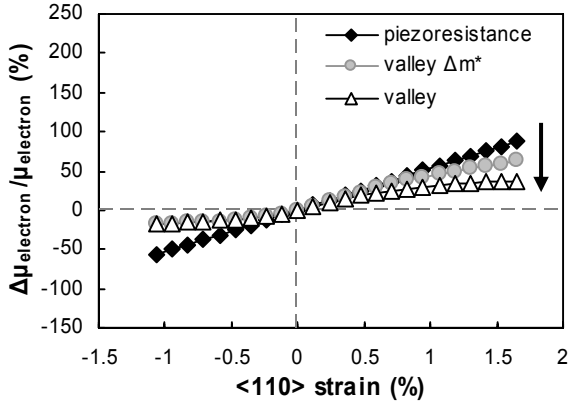

Figure 11: Change in electron mobility under <110> uniaxial strain for the classical piezoresistance model (18) and the valley-occupancy model (14) with and without effective mass change (Δm*).

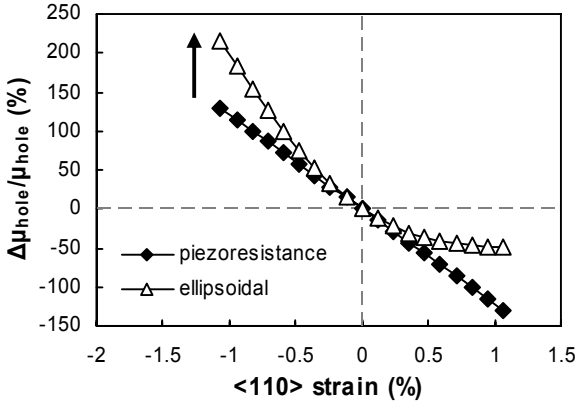

Figure 12: Change in hole mobility under <110> uniaxial strain for the classical piezoresistance model (18) and the ellipsoidal valence band modulation model (16).

Finally, the scaling behavior is analyzed by gate length reduction down to 20 nm and a roll-off behavior was found as shown in Figure 13. The strain-induced drive current enhancement initially increases for decreasing gate length down to a critical gate length of ~60 nm or ~45 nm for n-MOSFET with eSi:C and p-MOSFET with eSiGe, respectively. This is correlated to an increase in channel strain for smaller gate lengths. However, below a critical gate length, the drive current improvement starts to decline because the external resistance starts to dominate the total resistance and mobility gains have less impact on drive current. Parasitic resistance emerge as a new concern for short channel devices which leads to reduced drive current improvements despite increasing strain and mobility, making further scaling less rewarding. Beside this effect, p-MOSFET devices with eSiGe have the enormous advantage of a reduced S/D contact resistivity due to a lower valence band edge. This mitigates the detrimental impact of the parasitic S/D resistance and allows stressors to be effective again in deeply scaled p-MOSFET. An analogous effect of electron Schottky barrier height reduction in Si:C S/D was reported (22), but less effective dopant activation in Si:C (23) can offset this benefit.

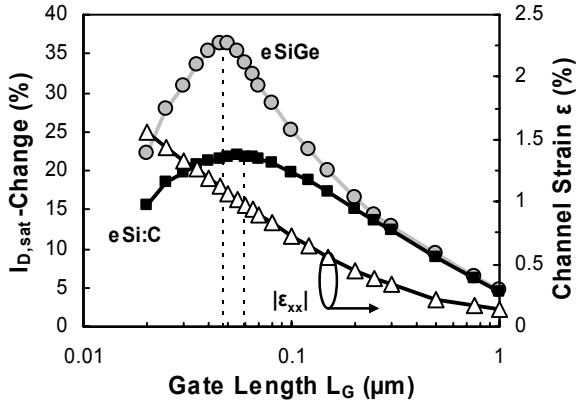

Figure 13: $I_{D,sat}$-gain vs. gate length rolloff for n-MOSFET with eSi:C and p-MOSFET with eSiGe, each compared to an unstrained reference. The lateral channel strain continuously increases for smaller gate lengths.

CONCLUSION

Process-induced strain from embedded S/D stressors like eSiGe and eSi:C is considered as a performance booster for current and future technology nodes. While eSiGe in p-MOSFET devices is widely adopted in industry, eSi:C for n-MOSFETs has not yet reached the maturity required for volume manufacturing. Mechanical stress simulations show for both types of embedded stressors an identical strain behavior related to changes in physical properties such as gate length, stressor depth, channel proximity, and alloy composition (at% Ge or at% C). This is expected because the integration approaches are similar. However, device simulations show significant differences between eSiGe and eSi:C in terms of how the strain is translated into drive current improvement. Non-linear relations between the channel strain and the carrier mobility lead to a super linear enhancement for holes while electrons suffer from saturation in mobility enhancement with increased strain. Higher strain levels from optimizations in strain engineering do not further improve n-MOSFET performance whereas simulations and experiments reveal a continuous p-MOSFET drive current enhancement. Beside this clear benefit for p-MOSFET devices, eSiGe has the enormous advantage of a reduced contact resistivity due to a lower valence band edge. However, in future nano scaled devices parasitic S/D resistance will be the performance limiter rather than the mobility-strain relation.

ACKNOWLEDGMENTS

This project was funded by the German Federal Ministry of Education and Research, registered under funding number 01M3167B and 13N9082. The author named in the publication bears responsibility for all published contents.

REFERENCES

1. M. Horstmann *et al.*, IEDM Technical Digest, 233-236 (2005).
2. M. Wiatr *et al.,* 15th Conference on Rapid Thermal Processing, 19-29 (2007).
3. K. Rim *et al.*, IEDM Technical Digest, 49-52 (2003).
4. Z. Ren *et al.*, IEEE Symposium on VLSI Technology, 172-173 (2008).
5. C. Auth *et al.*, IEEE Symposium on VLSI Technology, 128-129 (2008).
6. F.W. Voltmer and F.A. Padovani, Semicond. Silicon Mater. Sci. Technol., 75-82 (1973).
7. Y.-C. Yeo and J. Sun, Applied Physics Letters, 86, Issue 2, 023103 (2005).
8. G. Eneman *et al.*, IEEE Transactions on Electron Devices, 53-7, 1647-1656 (2006).
9. K.-J. Chui *et al.*, IEEE Transactions on Electron Devices, 54-2, 249-256 (2007).
10. G. Eneman *et al.*, IEEE Transactions on Electron Devices, 55-10, 2703-2711 (2008).
11. P.R. Chidambaram *et al.*, IEEE Transactions on Electron Devices, 53-5, 944-964 (2006).
12. K. Uchida *et al.*, IEDM Technical Digest, 129-132 (2005).
13. M. Berti *et al.*, Applied Physics Letters, 72-13, 1602-1604 (1998).
14. J.L. Egley and D. Chidambarrao, Solid-State Electronics, 36-12, 1653-1664 (1993).
15. E. Ungersboeck *et al.*, 11th Intern. Workshop on Comput. Electronics (IWCE), 141-142 (2006).
16. B. Obradovic *et al.*, 10th Intern. Workshop on Comput. Electronics (IWCE), 26-27 (2004).
17. Sentaurus Device User Guide A-2008.09, Synopsys Inc. (2008).
18. Y. Kanda, IEEE Transactions on Electron Devices, 29-1, 64-70 (1982).
19. M.L. Lee *et al.*, Journal of Applied Physics, 97-1, 011101 (2005).
20. S.E. Thompson *et al.*, IEDM Technical Digest, 221-224 (2004).
21. Y. Sun *et al.*, Journal of Applied Physics, 101, 104503 (2007).
22. M. Sinha *et al.*, Applied Physics Letters, 91, 242108 (2007).
23. Y. Liu *et al.*, IEEE Symposium on VLSI Technology, 44-45 (2007).