

SIMULATION OF ASYMMETRIC DOPED HIGH PERFORMANCE SOI-MOSFETS FOR VLSI CMOS TECHNOLOGIES

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ABSTRACT

Asymmetric halo and extension implantations are examined by simulation for their usability in 45 nm and 32 nm-technology high performance SOI-MOSFETs. Tilted implantations from the source side show higher saturation currents and lower drain overlap capacitances, which improve the intrinsic MOSFET power delay product. Furthermore the asymmetry leads to an inverter chain speed benefit. The stronger short channel effect, present in these devices, can be reduced by a low dose drain side halo implantation simultaneously maintaining a transistor performance improvement from asymmetric doping. This optimized transistor design is successfully transferred from the 45 nm into the 32 nm-technology.

INTRODUCTION

MOSFETs with asymmetric channel design are under evaluation since the nineties. The transistor used in (1) has lightly doped drain and source side halo implantations. A lower substrate current, higher punch-through voltage and less hot carriers are the results of this asymmetry. Further research in the next decade shows similar device behavior, but the focus there is on asymmetric halo or asymmetric extension implantations (2), (3). Symmetric MOSFETs, which are used for comparison in these investigations, have mainly uniform channel profile. The halo implantation inherently improves scalability of the asymmetric transistors. But performance enhancement can also be seen comparing with symmetric halo MOSFETs (4), (5). Some of the latest high performance transistors use asymmetric channels, however only with asymmetric halo or asymmetric extension implantations (6), (7). In this study either tilted single halo or tilted extension implantations and a combination of both are investigated. Symmetric MOSFETs with dual halo-implantations are used for comparison.

For the 45 nm technology, the static performance behavior is optimized by using different implantation settings. Furthermore the dynamic performance of asymmetric devices is compared to symmetric MOSFETs using the power delay product of single transistors and propagation delay time of inverter chains. Additionally the simulation results were highlighted with experimental data. The second part describes the impact of transistor scaling on the static and dynamic properties of asymmetric CMOS devices. For these purposes the 32 nm-technology with high-k gate dielectric and metal gate is used. The simulations were performed using Sentaurus TCAD from Synopsys. The quantum hydrodynamic transport model is used with a set of calibrated parameters.

45nm-TECHNOLOGY

SINGLE SIDE HALO IMPLANTATIONS

Asymmetric devices with single halo implantations from the source side (SSH) or from the drain side (DSH) are simulated. Figure 1 shows the doping concentration of a SSH n-type MOSFET. The halo implantation from one side leads to a slight reduction in the overlap of the implanted halo region, but there is almost no overlap capacitance difference between source and drain.

A higher channel doping concentration either on the drain or on the source side raises the electric field on the particular channel edge. Thereby SSH n-type MOSFETs have a higher electric field at the source side of the channel and a lower electric field at the drain side (Figure 2) and hence a higher averaged carrier velocity in the channel compared to symmetric devices (4).

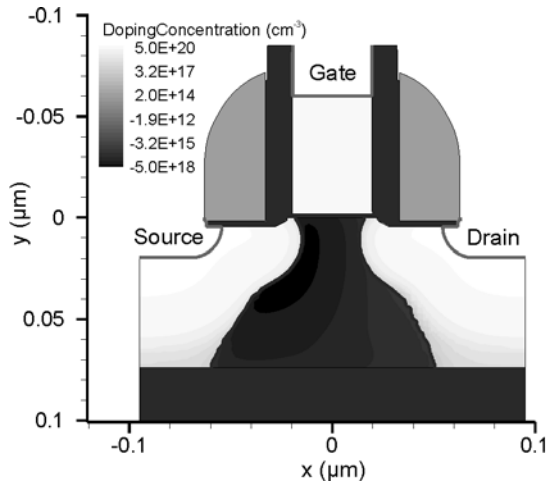


Fig. 1. Doping profile of a SSH n-type MOSFET

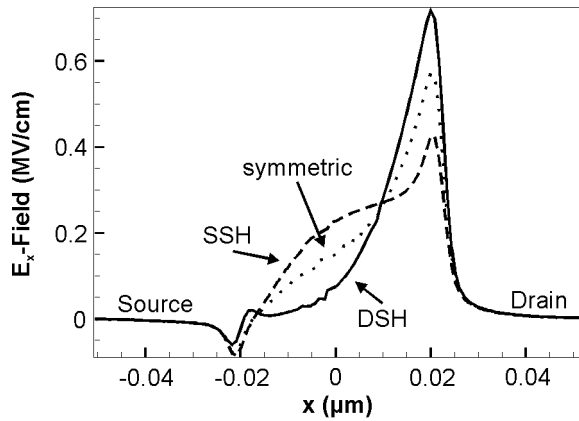


Fig. 2. Lateral electric field in the channel for symmetric and asymmetric n-type MOSFETs ($y = 3 \text{ nm}$)

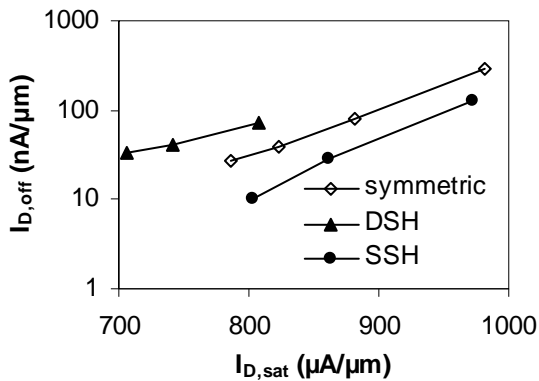


Fig. 3. Universal curve of single side halo n-type MOSFETs

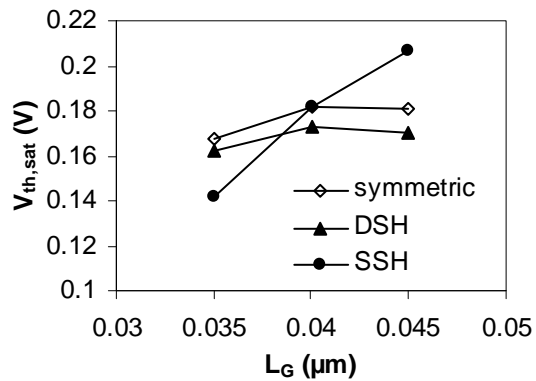


Fig. 4. Saturation threshold voltage roll-off of single side halo n-type MOSFETs

The universal curve (Figure 3) is about 6% improved for SSH MOSFETs. However, with a degraded saturation threshold voltage roll-off (Figure 4). On the other hand DSH-MOSFETs show universal curve degradation but no improved saturation threshold voltage roll-off. The saturation threshold voltage vs. varying gate lengths depends on the depletion zone penetration on the drain to the channel. Furthermore, DSH-MOSFETs have increased DIBL due to higher band-to-band tunneling on the drain side. For the p-type MOSFET the current improvement is in the same range as for the n-type MOSFET

SINGLE SIDE EXTENSION IMPLANTATION

Tilted extension implantations, as another way to generate channel asymmetry, are used to optimize the overlap and depth of the source and drain extension regions independently. Figure 5 shows the doping concentration 3 nm below the surface of the n-type MOSFET with a tilted source side extension implantation (tSSE). The doping in the drain extension is lower and the ambient halo is higher compared to the source side. The tilted second extension implantation degrades tremendously the universal curve behavior due to the under lap of drain side extension to the gate channel edge. A second extension implantation step without tilt and lower dose is introduced and reduces this under lap and improves the performance. The overlap capacitance varies about 100 aF/ μm between source and drain side channel overlap.

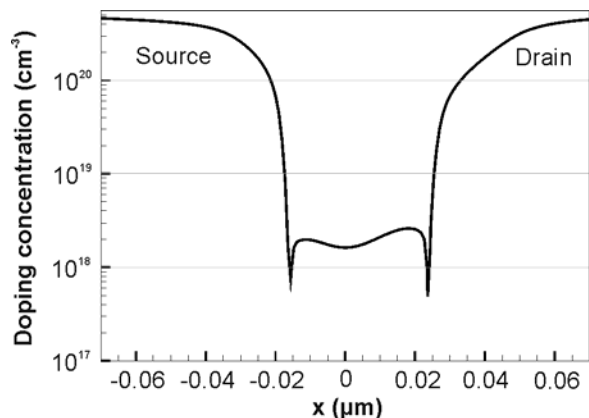


Fig. 5. Doping profile of a tSSE n-type MOSFET ($y = 3 \text{ nm}$)

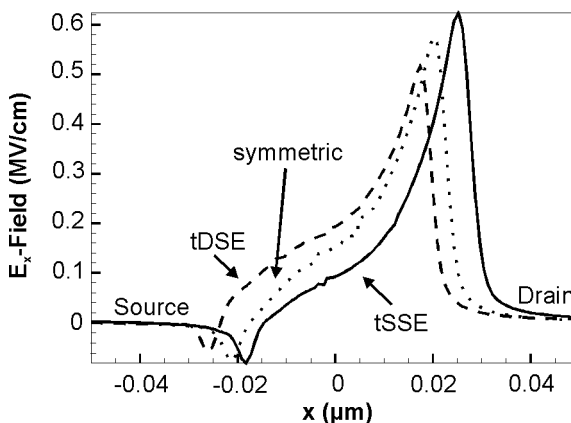


Fig. 6. Comparison of lateral electric field in the channel for symmetric and asymmetric n-type MOSFETs ($y = 3 \text{ nm}$)

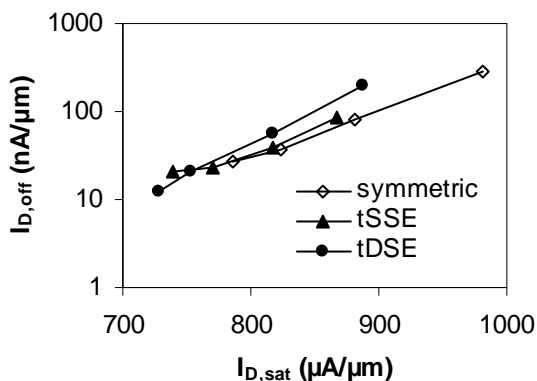


Fig. 7. Universal curve of single side extension implanted n-type MOSFETs

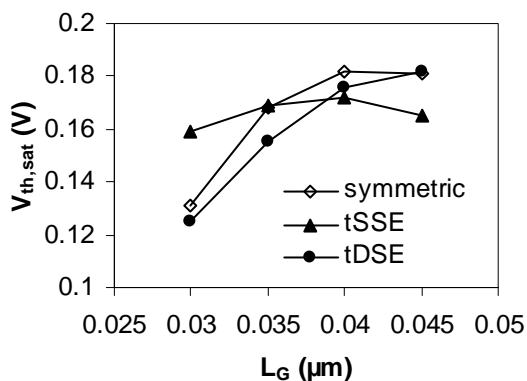


Fig. 8. Threshold voltage roll-off in saturation of single side extension implanted n-type MOSFETs

In the saturated MOSFET only the source side extension resistance influence the saturation current whereas the source and drain resistances affect the linear current. A smaller drain extension area with higher ambient halo doping reduces the saturation threshold voltage roll-off. Figure 6 shows higher lateral electric field at the source side of the channel for tilted drain side extension (tDSE) and here the drain current is increase. The field variations on the drain side have less influence on the drain current because the carrier velocity on this area is in saturation. Nevertheless the universal curve behavior (Figure 7) is degraded due to the source resistance, which is increased. The slightly degraded saturation currents of the tSSE MOSFETs suggest that the reduced source extension resistance did not compensate the

inappropriate electric field in the channel. Both implantation conditions lower the linear current due to a higher drain or source extension resistance.

The saturation threshold voltage roll-off of the tSSE benefits from the smaller drain side extension area and is improved (Figure 8). The tDSE n-type MOSFETs have a degraded threshold voltage behavior until 40 nm gate length caused by higher doped and larger drain extension region with less halo doping. Shorter gate lengths yield a beneficial doping distribution in the channel and improve the threshold voltage. The behavior of the p-type MOSFET is similar for the single side halos.

COMBINATION OF SOURCE SIDE HALOS AND SOURCE SIDE EXTENSIONS

The simulations of combined SSH and tSSE implantations, with the same conditions as in the previous sections, results in a comparable universal curve improvements for linear and saturation drive currents. Furthermore, a slightly better threshold voltage behavior than SSH is achieved, but still degraded compared to symmetric devices. The ratio between the source and drain side overlap capacitances is comparable to single side halo implantations. To reduce the extension resistance even further, the tilted source side extension (tSSEII) particularly the second source drain extension implantation (secSDEII) obtains higher implantation doses. The universal curve (Figure 9) is unchanged for the dose variation of the tilted implantation, but the non-tilted extension implantation with higher dose achieves 1% higher saturation drive current. The p-MOSFETs show a slightly lower universal curve improvement with similar threshold voltage roll-off. The modification of extension doping and depth has to be optimized due to the impact on short channel effects. The saturation threshold voltage roll-off degrades for higher extension implantation doses.

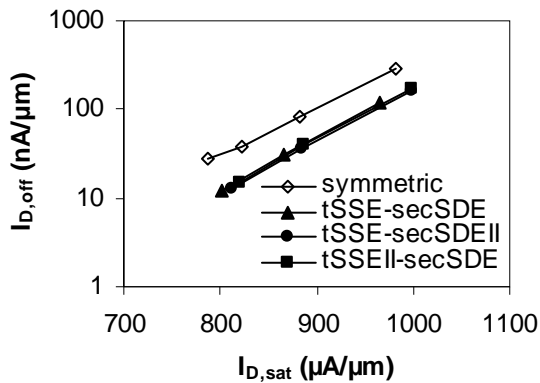


Fig. 9. Universal curve comparison of asymmetric SSH-tSSE n-type MOSFETs

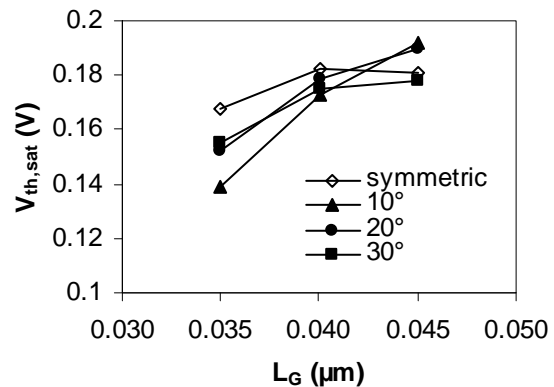


Fig. 10. Threshold voltage roll-off comparison and tilt variations of the drain side halo implantation

To improve the threshold voltage roll-off, an additional halo implantation step from the drain side (dDSH) with lower dose than the source side implantation was introduced. This step increases the doping around the drain extension area and reduces the drain depletion zone. On the other hand it has a negative impact on the lateral electrical field in the channel. Three different implantation angles (10°, 20°, 30°) with equal energy are simulated. Figure 10 shows better short channel behavior with increased tilt. The halo doping gets closer to the extension regions and moves into the channel, reducing the drain influence. The threshold voltage roll-off of the asymmetric n-type MOSFET is in a similar range of the symmetric n-type MOSFET for 30° tilt angle.

A tilt angle of 10° improves the universal curve by another 1% and a tilt angle of 30° shows a reduction by 0.5% (Figure 11). The higher channel and body doping degrades the saturation current and shows a decreased leakage current. The drain side halo implantation reduces the linear current starting with a tilt angle of 10° caused by the increasing drain extension resistance and it's in line with the symmetric

transistor for 30° tilt angle. The DIBL is unchanged for implantation tilts lower than 20° tilt angle and even more degraded for higher tilt angles due to a higher band-to-band tunneling rate.

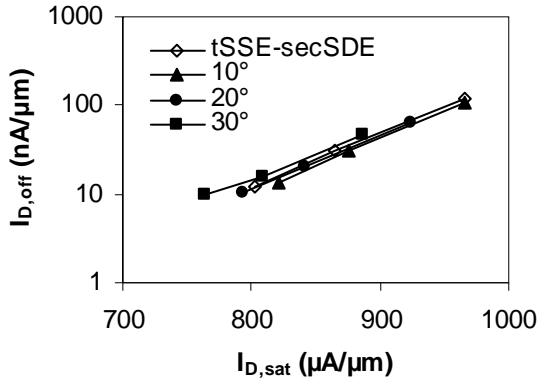


Fig. 11. Universal curve comparison incl. tilt variations of the drain side halo implantation of SSH-tSSE n-type MOSFETs

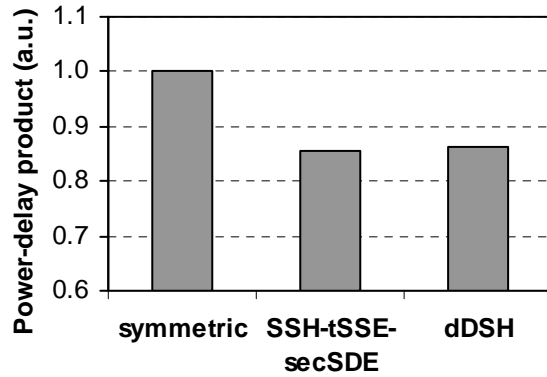


Fig. 12. Power delay product comparison between symmetric and asymmetric devices

Figure 12 compares the intrinsic power delay product between the symmetric and the combined asymmetric n-type MOSFET devices with $L_G = 40$ nm. Thereby, the asymmetry includes source side halo and tilted source side extension implantation with a second extension implantation (SSH-tSSE-secSDE) and additional DSH implantations with low dose (dDSH). The increase of the saturation current and the decrease of the gate-to-drain overlap capacitance reduce the power delay product for the combined asymmetric n-type MOSFET devices by about 15%. Both asymmetric options have identical improvements of 11% in the propagation delay time at a 100 nA static inverter current (Figure 13). Therefore, the propagation delay time of the second inverter in a three stage inverter chain is used. Experimental results show a ring oscillator speed benefit of 12 % and a universal curve improvement of up to 12%, which highlights the simulated transistor performance enhancements (8).

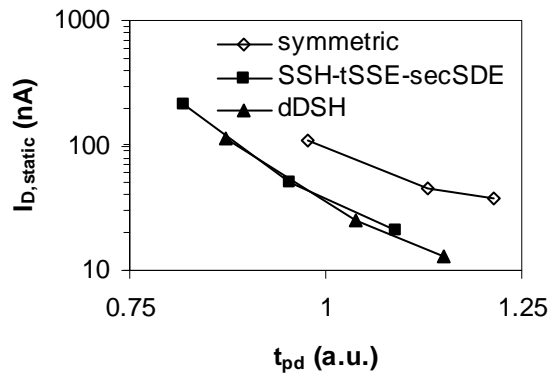


Fig. 13. Propagation delay time comparison between symmetric and asymmetric devices

32nm-TECHNOLOGY

To investigate the scalability of the asymmetric device design, MOSFETs with 30 nm gate length were simulated using high-k gate insulator and metal gate. The reduced capacitive gate oxide thickness and gate length in combination with changes in the process conditions result in a saturation current improvement compare to the symmetric design of the 45nm-technology.

Asymmetric devices in 32nm-technology contain a source side halo, a tilted source side extension and a second extension implantation (SSH-tSSE-secSDE) based on the 45nm-technology findings. Optionally a second halo implantation (dDSH) from the drain side is done to improve the short channel behavior. Figure 14 shows the doping concentration of the asymmetric device.

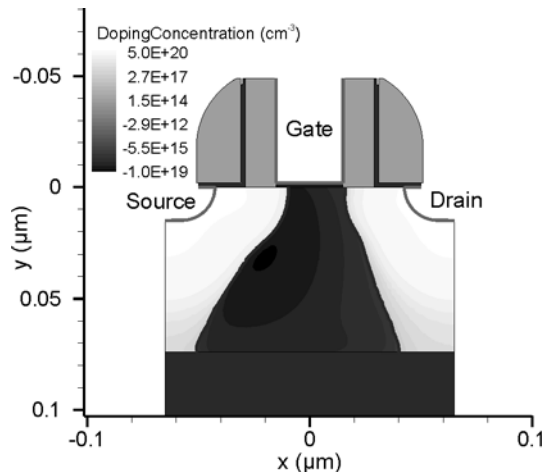


Fig. 14. Doping profile of a SSH-tSSE n-type MOSFET in 32nm-technology

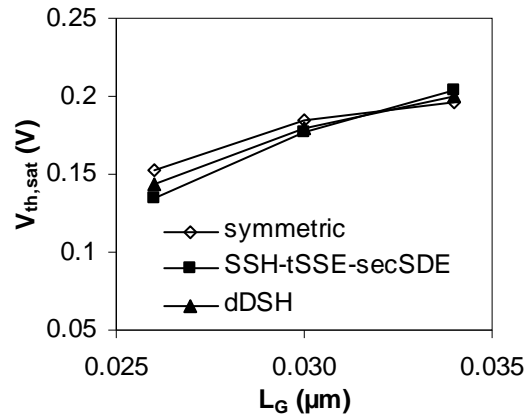


Fig. 15. Threshold voltage roll-off of the symmetric and optimized asymmetric n-type MOSFETs

Figure 15 contains the threshold voltage roll-off, which is only slightly degraded for the both asymmetric n-type MOSFETs. The additional halo implantation from the source side reduces the roll-off degradation. The universal curve in Figure 16 shows 3% improvement with the additional drain side halo implantation and 7% without it. In comparison with the threshold voltage roll-off, the SSH-tSSE-secSDE implantations should be preferred. Figure 17 clarify it where the device has 4% higher linear current at 100 nA leakage current with SSH-tSSE-secSDE. The p-type MOSFETs have slightly lower improvements. The static MOSFET characteristic of the 32 nm-technology shows the expected behavior and fits in well with the data of the 45nm-technology.

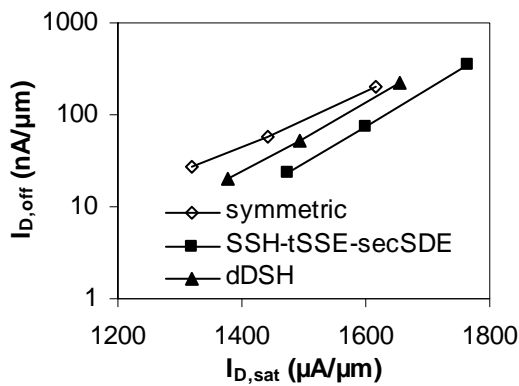


Fig. 16. Universal curve of the symmetric and optimized asymmetric n-type MOSFETs

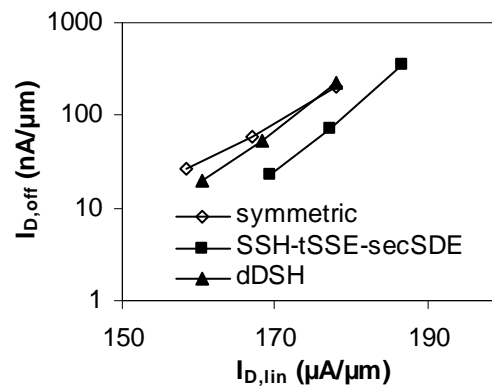


Fig. 17. Linear universal curve of the symmetric and optimized asymmetric n-type MOSFETs

The power delay product of the transistors with 30 nm gate length shows almost the same improvement up to 15% for combined asymmetric devices (Figure 18). The propagation delay time of the inverter chain is shown in Figure 19 and is 10% lower for the asymmetric MOSFET without the additional drain side halo implantation compared to the symmetric MOSFET. The dynamic improvements for asymmetric devices in 32nm-technology with optimized implant conditions are comparable to the 45nm-technology benefits.

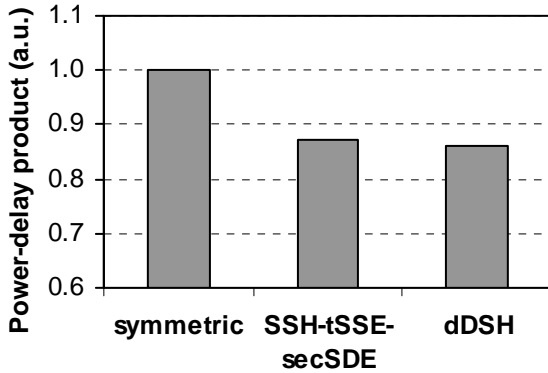


Fig. 18. Power delay product of the 32nm-technology n-type MOSFETs

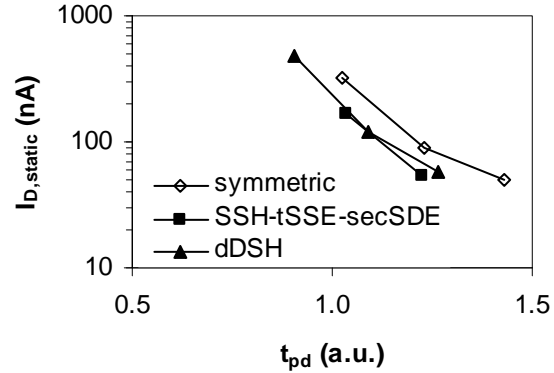


Fig. 19. Propagation delay time of the 32nm-technology n-type MOSFETs

CONCLUSION

Asymmetric MOSFETs with halo and extension implantation from the source side improve the universal curve behavior and the gate-to-drain overlap capacitance compared to symmetric devices. Due to asymmetric implantations the short channel behavior is slightly degraded. Additional halo implantation from the drain side are investigated and optimized to compensate those effects. The higher drive current and lower drain overlap capacitance reduces the power delay product up to 15% and the inverter propagation delay time about 11% for the 45nm-technology node. These improvements could be highlighted through experimental results of high performance PD-SOI-CMOS-FETs (8). Scaling to 32nm-technology, which includes high-k gate dielectric and metal gate, does not impact the advantages of the asymmetric transistor design. The behavior is slightly different caused by the diversified doping profile but can be optimized. The drive currents are improved up to 7% and the propagation delay times are 10% lower. Asymmetric MOSFETs with less channel doping at the drain side and highly doped source side extension areas are an attractive and challenging option for CMOS devices in current and future technology nodes.

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