Strained Isolation Oxide as Novel Overall Stress Element for Tri-Gate Transistors of 22nm CMOS and Beyond

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Abstract – This 3-D TCAD study demonstrates a new stress element by strained isolation oxide for Tri-Gate and similar FinFET structures. The simulation shows an uniform improvement of N- and PMOS drive current (10 %) by using a tensile strained isolation material between the fins processed on standard (100) bulk wafer with <110> channel direction. Therefore it is a simple low-cost stress method for Tri-Gate and FinFET structures of 22nm technologies and beyond. The main stress direction is located along the channel width with a maximum near the pn-junctions. The stress effect can be improved further with reduced gate length which shows the compatibility of strained isolation oxide to future transistor generations.

Introduction: In order to achieve enhanced gate control for transistors of 22nm technologies and beyond, investigations have been made for successful and low-cost integration of Tri-Gate structures into existing planar CMOS processes [1,2]. However, continuing scaling and a complex Tri-Gate geometry don't allow the usage of conventional dual stress liner (DSL) [3]. The most powerful stress element is the embedded SiGe of PMOS.
This study presents a novel stress element for Tri-Gate structures of 22nm CMOS which is achieved by strained isolation oxide between low-profile fins and provides an uniform performance improvement of N- and PMOS. The results are based on 3-D simulations around 22nm technology ground rules in line with ITRS assumptions and give an idea of the ability to use stress for Tri-Gate or other FinFET structures in future scaling.

Results and Discussion: The simulated Tri-Gate structure was realised by a planar 22nm CMOS process (L_{gate} = 26 nm, EOT = 1.0 nm) and an additional mask, etch, and deposition step to create the Tri-Gate fin with H_{Fin} = 10 nm, W_{Fin} = 20 nm and a distance between the fins of P_{Fin} = 50 nm (Fig. 1).

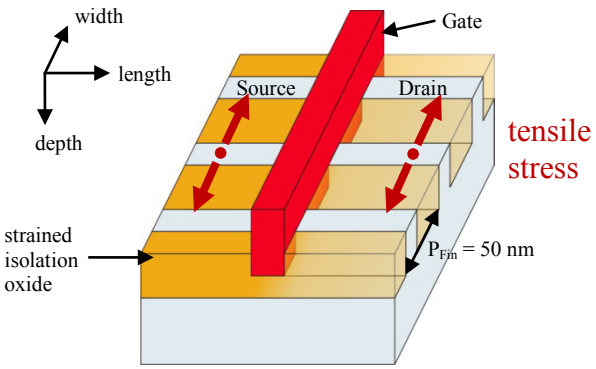

Fig. 1: *Tri-Gate structure with strained isolation oxide between low-profile fins.*

Following the fin formation, planar and Tri-Gate MOSFETs used the same workfunction metal, implants and epitaxial S/D to obtain a nearly identically doping profile [2]. The isolation oxide (shallow trench isolation, STI) is mainly used to eliminate the parasitic gate capacitance around the lowered side gate and can be processed to achieve an intrinsic tensile or compressive stress [4]. In this case we used silicon oxide, but it should be possible to create the STI of fins by plasma enhanced nitride (PEN) as used for DSL. Figure 2 illustrates the stress profile along the width of a Tri-Gate transistor (1 GPa tensile stressed isolation oxide) which is the most dominating stress direction due to the counteraction of each fin that prevents the relaxation of the stressed isolation oxide. The maximum stress value could be observed near the pn-junction because the amorphisation by the extension implantation.

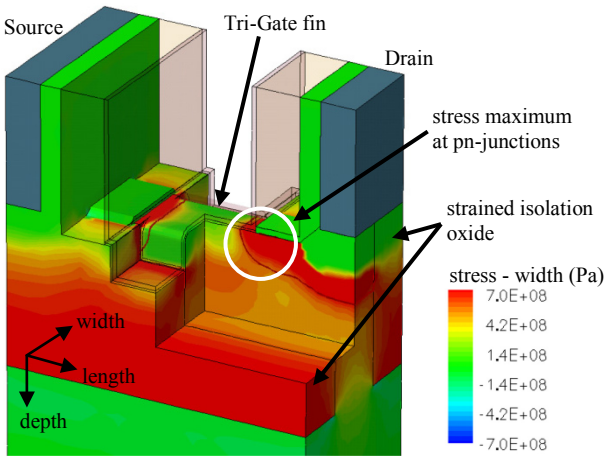

Fig. 2: *Simulated stress profile of N-Tri-Gate transistor width direction with maximum at pn-junctions.*

During the replacement gate process the center of Tri-Gate fin relaxes which could be compensated in future technologies by metal gate stress [5]. The stress in channel length is clearly smaller due to the minor volume of isolation oxide compared with the bulk material below and its direct interface. After fin formation the isolation oxide is exposed at top all over the transistor length and can totally relax along the depth direction whereby no stress of this component is coupled into the fin (Tab. 1).

Tab. 1: *Average channel stress for different oxide stress.*

Type	simulated isolation oxide stress (GPa)	average stress (MPa)		
		length	depth	width
NMOS	0	-2	0	1
	1	**216**	**3**	**367**
	-1	-223	-5	-357
PMOS	0 (eSiGe 35%)	-1934	87	192
	0 (eSiGe 27%)	-1524	71	163
	1 (eSiGe 35%)	**-1573**	**71**	**620**
	-1 (eSiGe 35%)	-2315	94	-253

With 1 GPa tensile strained isolation oxide the NMOS transistor shows a performance improvement of drain current by 12 % (Fig. 3). The increased mobility is received from the tensile stress in length and width direction of the Tri-Gate fin which affect the in-plane conduction band valleys near the top-gate where the most carriers are located. The conduction band energy of this in-plane valleys increase with tensile stress and results in a redistribution of electrons into out-of-plane valleys with smaller effective mass and higher electron mobility. Therefore a -1 GPa compressive isolation leads to a degradation of drain current.

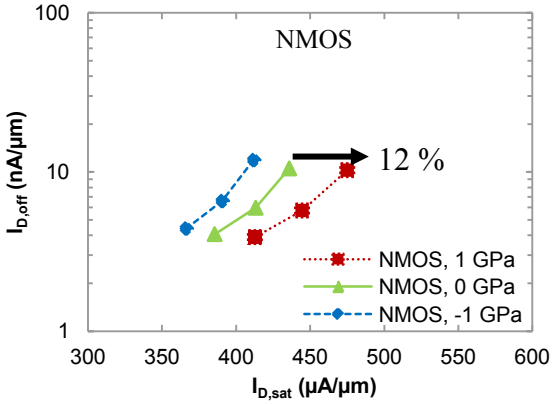

Fig. 3: *$I_{D,off}$ to $I_{D,sat}$ normalized to effective gate width for N-Tri-Gate transistors with strained (1 GPa tensile, -1 GPa compressive) and unstrained isolation oxide (H_{Fin} = 10nm, W_{Fin} = 20 nm, L_{gate} = 22 - 30 nm).*

A very positive effect is the similar performance behaviour of PMOS transistors in combination with eSiGe. Figure 4 illustrates a total drain current improvement by 9 % with a 1 GPa tensile strained isolation oxide and 35 % Germanium of the embedded SiGe. The length direction of Tri-Gate fin provides the dominant compressive stress values due to embedded SiGe. The tensile stress component of the isolation oxide in length direction indeed leads to a drain current degradation and a shift of the maximum valence band edge resulting in higher threshold voltage of approximately 20 mV shown in Table 2.

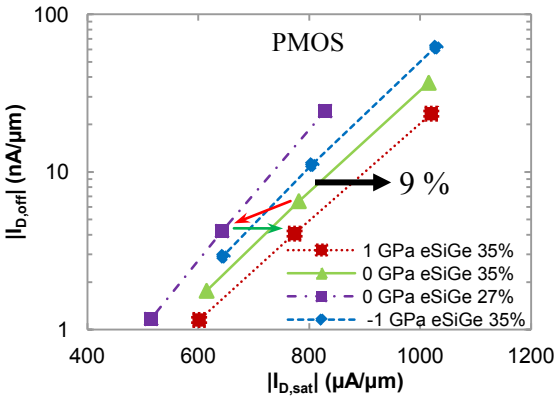

Fig. 4: *$I_{D,off}$ to $I_{D,sat}$ normalized to effective gate width for P-Tri-Gate transistors with eSiGe and strained (1 GPa tensile, -1 GPa compressive) and unstrained isolation oxide (H_{Fin} = 10nm, W_{Fin} = 20 nm, L_{gate} = 22 - 30 nm).*

The PMOS values with 27 % Germanium and an unstrained isolation oxide are used to demonstrate the performance with a comparable stress component in length direction (-1.5 GPa, Tab. 1) but without the oxide stress of width direction (red arrow, Fig. 4). This degradation can be more than compensated by the 450 MPa tensile oxide stress in fin width direction (green arrow, Fig. 4) without a shift of threshold voltage because the stress component in length direction is still the dominating one for the valence band maximum and the resulting bandgap.

Tab. 2: *PMOS threshold voltage for different oxide stress.*

Type	oxide stress (GPa)	$V_{th,lin}$ (V)	$V_{th,sat}$ (V)
PMOS	0 (eSiGe 35%)	-0.267	-0.214
	0 (eSiGe 27%)	-0.283	-0.228
	1 (eSiGe 35%)	**-0.284**	**-0.230**
	-1 (eSiGe 35%)	-0.248	-0.197

Figure 5 shows the channel stress along the width direction as a function of the physical gate length. The stress value around the pn-junction remains relatively unchanged while center and average stress increase with smaller gate length. That is a very important aspect because the most known stress mechanism like DSL, stress memorisation techniques (SMT) or contact metal stress are limited to larger structures and lose their effect or cannot be integrated in sub 22nm technologies due to the small transistor pitch and the limited contact area. This behaviour demonstrates the ability to use strained isolation oxide for the next FinFET technology nodes. The center and average stress values can also be increased by shrinking the gate length and approach to the 1 GPa stress of isolation oxide.

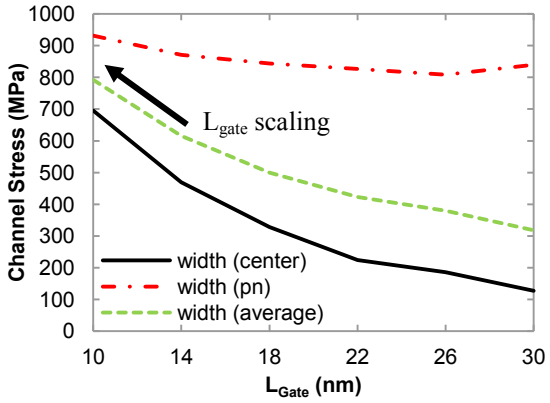

Fig. 5: *Channel stress along width direction as function of the physical gate length (1 GPa strained isolation oxide). Average is the mean value over the channel length.*

The induced channel stress in width direction can also be illustrated in dependence of intrinsic oxide stress (Figure 6). Any part of the N-Tri-Gate fin shows a linear behaviour and suggests the ability of additional superposition with other stress techniques which could be previously observed for DSL of planar CMOS transistors. The channel stress at the pn-junction has an increase of 0.7 what reflects a straight transition of intrinsic oxide stress into the silicon fin. The P-Tri-Gate transistor with embedded SiGe shows same behaviour and also confirmed the linear superposition with other stress elements.

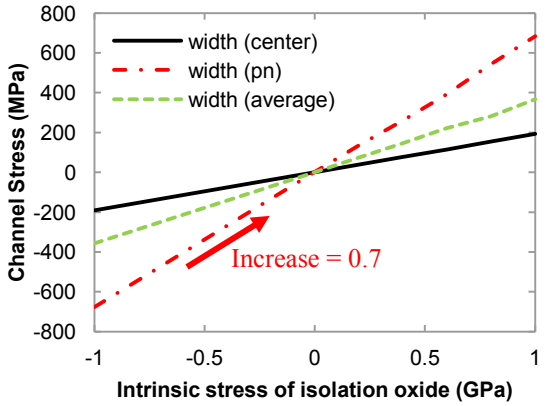

Fig. 6: *Channel stress along width direction as function of the intrinsic stress of isolation oxide (L_{gate} = 26 nm).*

Another important parameter is the pitch of the fins P_{Fin} which consists of Tri-Gate width and the distance between two fins. The stress in width direction is the main component and changes with the available space for the strained isolation oxide. Figure 7 illustrates the correlation between channel stress and fin pitch of a Tri-Gate transistor with 20 nm fin width. The channel stress increases with fin pitch until P_{Fin} = 50 nm, after that the stress values begin to saturate and an further increase of fin pitch brings no further advantage. More distance between two fins means less space for Tri-Gate fins at the same active area and less total drive current of transistor. For greater fin pitch it is necessary to increase also the fin height because the effective gate width consisting of the fin width and two times fin height should be more than the fin pitch.

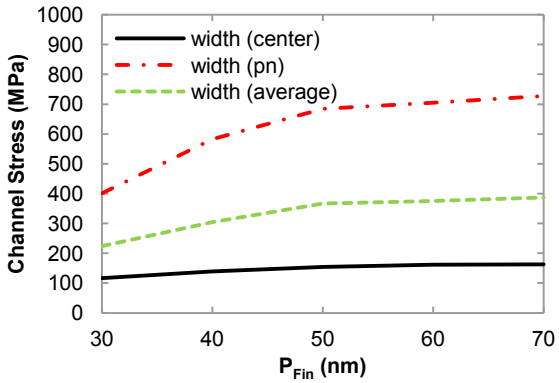

Fig. 7: *Channel stress along width direction as function of the fin pitch (L_{gate} = 26 nm, W_{Fin} = 20 nm).*

Conclusion: A low-profile Tri-Gate transistor with strained isolation oxide as new stress element with the potential for future technology nodes has been investigated. N- and PMOS show a similar performance improvement of drain current (9 - 12 %) by using tensile strained oxide between the fins. Transistor width is the main stress direction with the highest value around the pn-junction. The stress effect can be improved by shrinking the gate length and is linear dependent from the intrinsic oxide stress. Thereby, this stress method gives a low-cost and easy to implement opportunity to use mechanical stress for Tri-Gate and FinFET structures in future CMOS technologies.

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