Impact of Solid Phase Epitaxial Regrowth on Device Performance for Non-Diffusive Flash-Annealed 45nm SOI-MOSFETs

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In a standard process with a conventional rapid thermal annealing (RTA) stress engineering is a standard feature for advanced CMOS technologies to improve device performance [1]. Unfortunately, such an annealing scheme does not meet the 32 nm node requirements due to thermal diffusion and solid solubility limitations. To solve the problem, technologies like flash lamp annealing (FLA) [2], laser annealing [3], and solid phase epitaxial regrowth (SPER) [4] have been intensively investigated as an alternative to RTA. Stress techniques like embedded SiGe (e-SiGe) and dual stress liner (DSL) are already implemented on diffusionless SOI-CMOS devices successfully as shown in Figure 1. In [5], a new stress memorization technique (SMT) is used to induce tensile stress into the channel using a low temperature SPER process. The temperature for this stress memorization phenomenon is usually below 700°C and therefore, a negligible amount of dopant diffusion occurs. Thus, this stress technique could be also a method to enhance performance of a diffusionless n-MOSFET device further. This report shows for the first time the impact of an additional low temperature SPER annealing on device performance of non-diffusive flash-annealed MOSFETs.

To evaluate the stress effects, these experiments were run on both n- and p-MOSFET. Two splits are investigated: a FLA only reference device and a low temperature SPER+FLA device. Because this SMT requires an amorphized source/drain region and a capping layer the SPER annealing was added after the layer deposition for spacer formation. All the other process parameters were chosen to be identical for all of these two splits. The FLA for both devices was performed before silicidation. The TEM cross-section of a 35 nm device is represented in Figure 2.

Figure 3 shows the I_{on}/I_{off} characteristics obtained with the FLA only and SPER+FLA devices for n- and p-MOSFET. In contrary to the performance gain for n-MOSFET in ref. [5], a 6 % I_{on} degradation is observed for the SPER+FLA devices. We assume that the stress memorization phenomenon for the n-MOSFET is overlaid by other effects. In order to investigate the possible origin of the degradation, several parameters were monitored. Figure 4 shows the SDE sheet resistance (R_s) for n- and p-MOSFET of the FLA only and the SPER+FLA devices measured on dedicated test structures located next to the transistor test structures. A much higher R_s is apparent for the SPER+FLA devices in comparison to the FLA only devices (+ 200 % for n-MOSFET, + 50 % for p-MOSFET). We believe that this effect is a deactivation or an insufficient activation problem of the SDE due to the combined SPER annealing and FLA. This result indicates that for n- and p-MOSFET the observed I_{on} degradation of the SPER devices is mainly driven by SDE resistance. Figure 5 shows the source-drain to gate overlap capacitance. A 30 aF overlap capacitance difference between the FLA only and SPER+FLA devices for n-MOSFET (20 aF for p-MOSFET) can be observed. This corresponds to an enhanced lateral diffusion of 1.4 nm for the n-MOSFET (1.0 nm for p-MOSFET). We think this effect is caused by transient enhanced diffusion (TED) of the source-drain implants during the following high temperature FLA. Correcting this shift in gate-to-drain overlap, we would expect another 5% performance loss for the SPER+FLA devices.

In conclusion, it could be shown that with FLA only in comparison to the combination of SPER and FLA less lateral diffusion and better I_{on}/I_{off} performance for n- and p-MOSFET can be achieved. In addition, for the combination of SMT and FLA in a diffusionless SOI-MOSFET device more investigation is required to improve device performance further.

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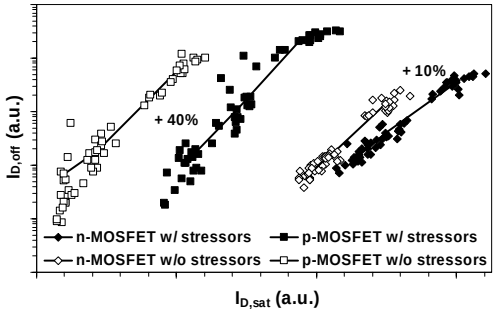

Figure 1: Ion/Ioff characteristics for n- and p-MOSFET with and without stressors (n-MOSFET: tensile stess liner, p-MOSFET: e-SiGe and compressive stress liner).

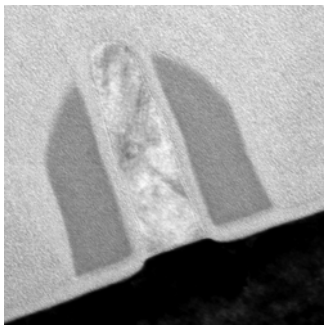

Figure 2: TEM cross-section of a L_G = 35nm device.

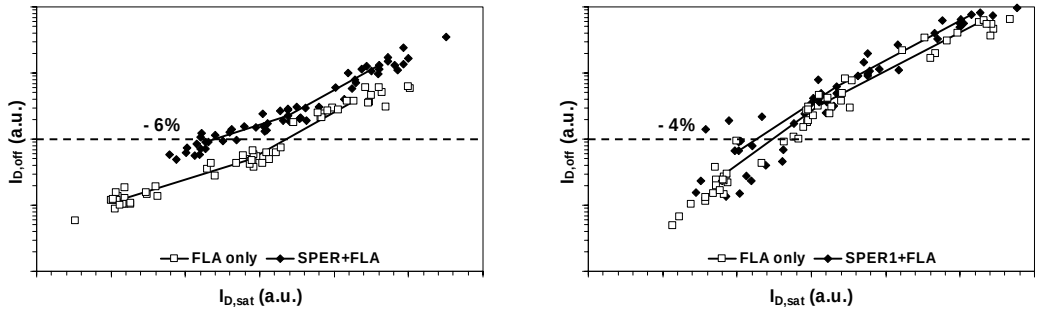

Figure 3: Ion/Ioff characteristics for the FLA only (squares) and the SPER+FLA devices (full diamonds), left – n-MOSFET, right – p-MOSFET.

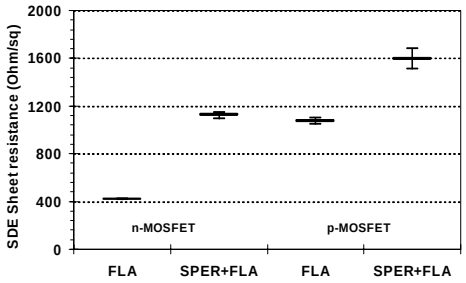

Figure 4: Comparison of the SDE sheet resistance of the FLA only devices and SPER+FLA devices, for n- and p-MOSFET.

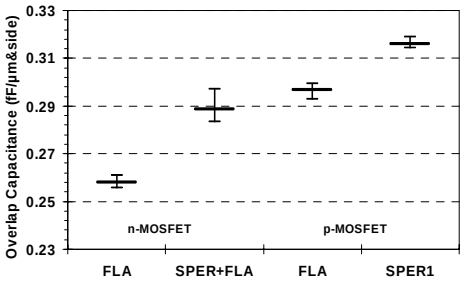

Figure 5: Comparison of the Overlap capacitance of the FLA only devices and SPER+FLA devices, for n- and p-MOSFET.