Student Paper

Study of 22/20nm Tri-Gate Transistors Compatible in a Low-Cost Hybrid FinFET/Planar CMOS Process

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Introduction: For future scaling to the end of the ITRS roadmap, novel structures like FinFETs are required to improve electrostatic integrity of MOSFETs with gate lengths shorter than 35 nm [1-4]. Classic fully-depleted FinFETs with a high aspect ratio are not compatible with existing planar process flows. A Tri-Gate transistor has the advantage of being more compatible. It is even possible to produce low-profile Tri-Gates in parallel to planar MOSFETs [5], with shared Tri-Gate and planar implants and common-use of source/drain epi and dual band-edge metal gate workfunctions. This maintains the design flow, saves mask count, allows reuse of analog and high-voltage I/O designs, while exploiting Tri-Gates in high speed logic and low minimum voltage.

Results and Discussion: To demonstrate this concept, a planar CMOS process was first simulated in 3-D around 22 nm technology ground rules with an assumed nominal L_{gate} = 26 nm and EOT = 1.0 nm, in line with ITRS assumptions. The planar MOSFET 3-D process simulation was then extended by an additional mask, etch, and deposition step to create a Tri-Gate structure, as shown in Fig.1. Following the fin formation, planar and Tri-Gate MOSFETs are running the same process in terms of implants and epitaxial S/D. The resulting dopant profiles in the Tri-Gate transistor are nearly identical to that of the planar process. Tri-Gate transistors with 20nm fin width and 10nm high side gates have significantly better gate control and show significant improvement of DIBL and subthreshold slope (sat.) from 92 mV/dec to 73 mV/dec (NMOS, Fig.2) and from 95 mV/dec to 77 mV/dec (PMOS). This translates into an effective EOT reduction in the Tri-Gates, and thus effectively reduces random doping fluctuation (RDF). Due to the improved electrostatics of the low-profile halo-doped Tri-Gate, halo dose to be further reduced while maintaining subthreshold slope as shown in Fig. 3, for additional improvement in RDF. This improvement in electrostatics can translate into Lgate scaling as well. The significance of the enhanced electrostatic behavior of Tri-Gates is further illustrated in Fig. 4. Planar MOSFETs show a clear V_T-rolloff to sub-nominal while Tri-Gate rolloff curves remain almost flat.

The low-profile halo-doped Tri-Gate exhibits a lower threshold voltage caused by improved subthreshold slope and a high electron density at the corners due to corner effects [6]. There are two relevant solutions to suppress corner effects and for retargeting of Tri-Gate threshold voltage. The first is a corner rounding process, which is already induced by process cleaning steps. Another solution requires an additional corner implantation which is self-aligned to Tri-Gate corner regions via fin formation nitride hardmask, and allows a homogenous counter doping over the whole gate length.

Optimization of fin geometry is studied by a variation of fin height (0 - 50 nm) and width (15 - 30 nm). Starting from the planar limit, segmentation of the active area into W_{Fin} and addition of gate wrap-around with H_{Fin}, the subthreshold slope decrease and shows a saturation at H_{Fin} = 10 nm.

With a planar-like extension/halo dopant profile, higher fins have also a worse behavior of $I_{D,off}$ and $I_{D,sat}$ due to series resistance. Fig. 5 demonstrates that a fin height of 7 nm and width of 20 nm is the optimal Tri-Gate geometry, where 7nm matches the extension junction depth. A narrow fin less than 15 nm becomes fully-depleted and is not useful for a hybrid CMOS process as it requires another gate metal workfunction to maintain positive V_T, and is thus no longer compatible with co-processed planar transistors. The stability of threshold voltage and subthreshold slope depending on process variations (H_{Fin} or $W_{Fin} \pm 4$ nm) is shown by Fig. 6. H_{Fin} is the most critical parameter and must be very well controlled in process.

Conclusion: A low-profile extension/halo-doped Tri-Gate which is compatible to a planar process has been evaluated and shows significant electrostatic and drive current benefits compared to planar. This is maintained over a large design space of Tri-Gate fin width and height. Such a Tri-Gate is the basis for a

low-cost Tri-Gate/planar hybrid technology, where Tri-Gates and planar would share the same implant masking, same S/D processes, and same dual band-edge metal gate workfunctions. In such a technology, planar transistors could be run at longer channel lengths to support analog and high voltage I/O, while Tri-Gates would be run in low-voltage SRAM and high speed logic.

References:

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[3] K. Okano et al. "*Process Integration Technology and Device Charact...*", IEDM Tech. Dig. 2005, pp. 721-724
[4] C.Y. Chang et al. "*A 25-nm Gate-Length FinFET Transistor Module for...*", IEDM Tech. Dig. 2009, pp. 293-296
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[6] B. Doyle et al. "*Tri-Gate Fully-Depleted CMOS Trans...*", VLSI, Dig. of Tech. Papers, pp. 133-134, June 2003
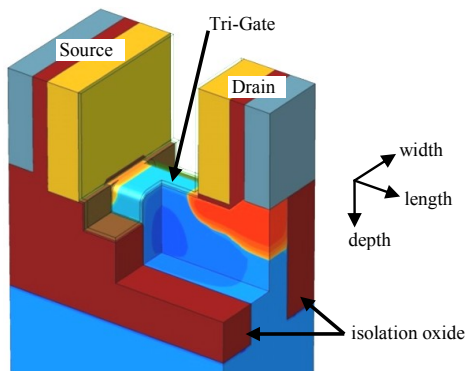
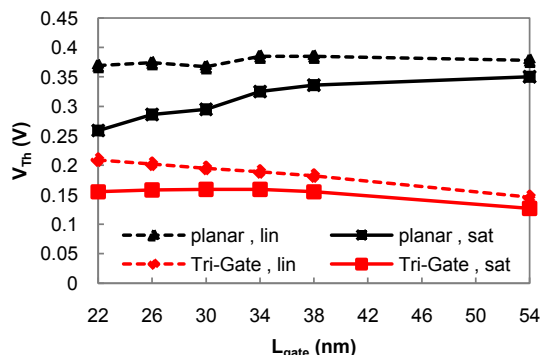**Fig. 1:** *Simulated n-Tri-Gate transistor cut at the half Tri-Gate transistor width and length.*

Fig. 4: *Simulated roll-off curve for a planar and Tri-Gate NMOS (H_{Fin} = 10nm, W_{Fin} = 20 nm)*

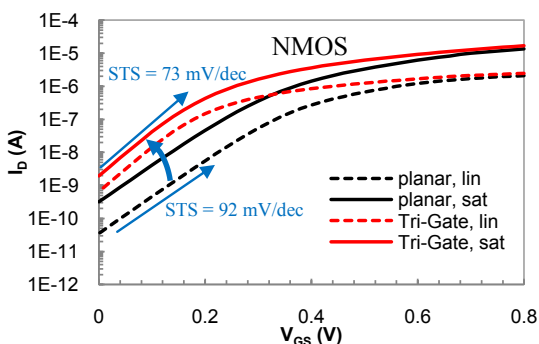**Fig. 2:** *Transfer characteristic (log.) for a planar and Tri-Gate NMOS (H_{Fin} = 10nm, W_{Fin} = 20 nm, L_{gate} = 26 nm)*
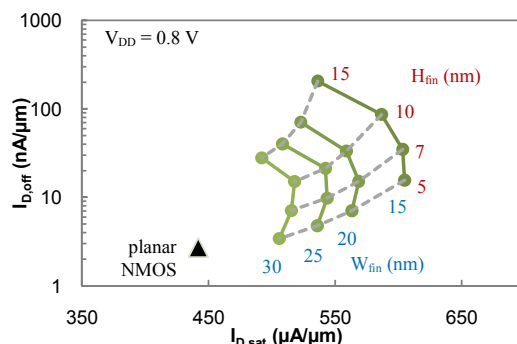

Fig. 5: *$I_{D,off}$ to $I_{D,sat}$ normalized to total gate width for different widths and heights of Tri-Gate NMOS (L_{gate} = 26 nm)*
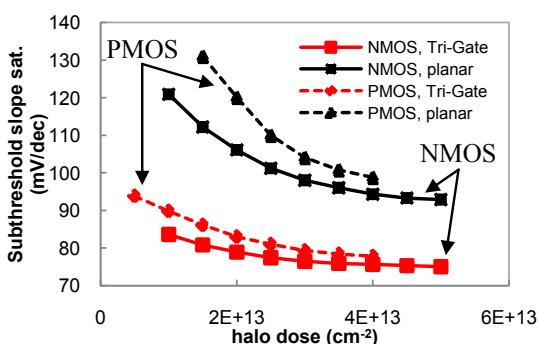

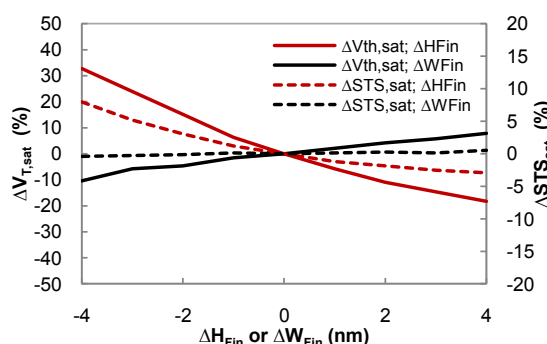**Fig. 3:** *Subthreshold slope of planar and Tri-Gate N- and PMOS as a function of halo dose (L_{gate} = 26 nm)*

Fig. 6: *Percent change of NMOS threshold voltage and subthreshold slope depending of ΔH_{Fin} or ΔW_{Fin}. Note that PMOS looks similar. (H_{Fin} = 10nm, W_{Fin} = 20 nm, L_{gate} = 26 nm)*