Simulation and Optimization of CMOS-Transistors for RF-Applications

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Abstract

The integration of CMOS logic circuits with RF components in the same technology opens new capabilities and reasonable solutions. Hence the investigation of consisting CMOS technologies for RF application and their optimization is a special field of interest.
In the paper n- and p-channel MOSFETs of a 0.35µm CMOS process are simulated by a two-dimensional numerical method. The static as well as the dynamic simulation results of the basic structures show a good agreement with experimental values. The cut-off frequencies are f_{max} = 47 GHz and f_T = 32 GHz for the n-MOSFET and f_{max} = 21 GHz and f_T = 13 GHz for the p-MOSFET. For the determination of the influence of tolerances in the technology process and for the device optimization different structure parameters are varied and the effects on static and RF behavior are represented. Furthermore methods for determination of small-signal equivalent circuits are discussed.

Kurzfassung

Die Integration von CMOS-Logik-Schaltungen zusammen mit HF-Komponenten in einer Technologie eröffnet neue Möglichleiten und kostengünstige Lösungen. Daher ist die Untersuchung von bestehenden CMOS-Technologien auf HF-Tauglichkeit sowie eine diesbezügliche Optimierung von besonderem Interesse.
Im Beitrag werden n- und p-Kanal MOSFETs einer 0.35µm-CMOS-Technologie mit Hilfe einer zweidimensionalen numerischen Methode simuliert. Die Ergebnisse der statische und dynamische Simulation zeigen eine gute Übereinstimmung mit experimentellen Ergebnissen. Die Grenzfrequenzen betragen f_{max} = 47 GHz und f_T = 32 GHz für den n-MOSFET bzw. f_{max} = 21 GHz und f_T = 13 GHz für den p-MOSFET. Zur Ermittlung der Einflüsse der Toleranzen des Technologieprozesses sowie zur Optimierung der Bauelemente wurden verschiedene Strukturparameter variiert und der Einfluss auf das statische und HF-Verhalten bestimmt. Weiterhin werden Methoden zur Bestimmung der Kleinsignalersatzschaltungen diskutiert.

1 Introduction

The permanent growth of communication technologies requires integrated circuits with increasing operating velocities and cut-off frequencies. Particularly in wireless communication systems CMOS-circuits for RF-applications are requested to achieve convenient system solutions and high product volumes at low cost. The integration of CMOS logic circuits with RF components in the same technology opens new capabilities and reasonable solutions. Hence the investigation of consisting CMOS technologies for RF application and their optimization is a special field of interest. Therefore systematic simulation of n- and p-channel MOSFETs of a 0.35µm CMOS process are carried out
In Section 2, the simulation model is described. The DC- and RF-simulation results of n- and p-channel MOSFETs and the comparison with experimental results are presented in Section 3. Section 4 shows results of the variation of technological parameters for an optimization of the structures.

2 Simulation Model

The numerical simulation is carried out by the 2D/3D-simulator SIMBA [1-3], based on a two- or three-dimensional coupled solution of
Poisson equation

$$\nabla \cdot (\varepsilon \nabla \varphi) = -e(p - n + N_D^+ - N_A^-)$$

(N_D^+, N_A^- ionized donor and acceptor densities)

the continuity equations for holes and electrons

$$\nabla \cdot \mathbf{J}_p = -e \cdot (R - G + \partial p / \partial t)$$
$$\nabla \cdot \mathbf{J}_n = e \cdot (R - G + \partial n / \partial t)$$

($\mathbf{J}$ current density, R recombination rate, G generation rate)

and the corresponding transport equations

$$\mathbf{J}_p = -e\mu_p p \nabla \varphi - kT\mu_p \nabla p$$
$$\mathbf{J}_n = -e\mu_n n \nabla \varphi + kT\mu_n \nabla n$$

(μ_p, μ_n hole and electron mobilities).

Additionally the heat flow equation and the energy balance equations for holes and electrons can be included for a further refinement of the physical model. These extended models increase the simulation effort considerably, so only a few calculations for validation have been done.
From the results of the static and dynamic simulations the y-parameters as a function of frequency can be calculated. From this the high-frequency parameters small-signal current gain (h_{21}), maximum stable gain (MSG) and maximum available gain (MAG) can be derived, which yield the corresponding cut-off frequencies the transit frequency (f_T) and the maximum frequency of oscillation (f_{max}). Furthermore the parameter of the small-signal equivalent circuit can be calculated. By inclusion of the bulk terminal the corresponding substrate elements are ascertainable.

3 Results and Verification

The p- and n-channel-MOSFET-structure including the bulk terminals used for the simulations is represented in **Fig. 1**. The typical gate length is 0.35 µm and the structure width amounts 20 µm. The doping profiles of the implantation process result from previous process simulations and from

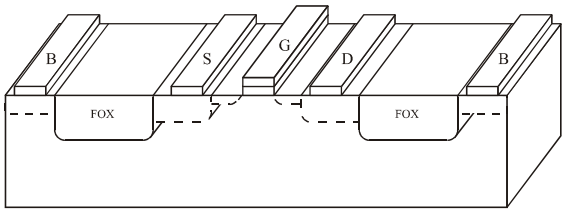

Fig. 1 MOSFET-structure used for simulations

measurements. As an example the impurity densities of the n-channel-LDD-regions are plotted in **Fig. 2**.

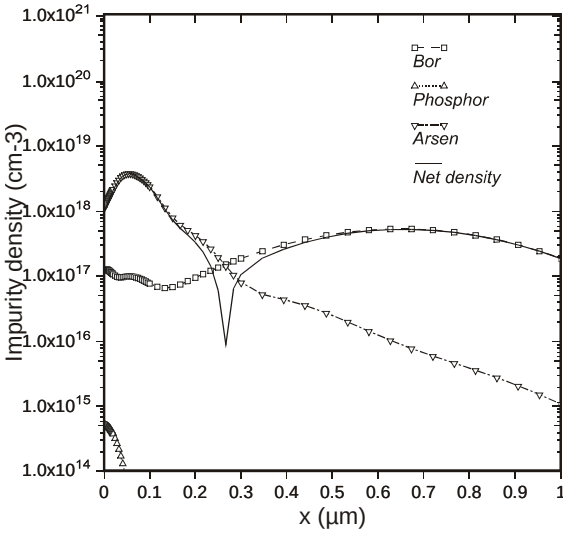

Fig. 2 Impurity densities of the n-channel-LDD-regions

The calculated output characteristics of the n- and the p-MOSFET are represented in **Fig. 3** and **Fig. 4**.

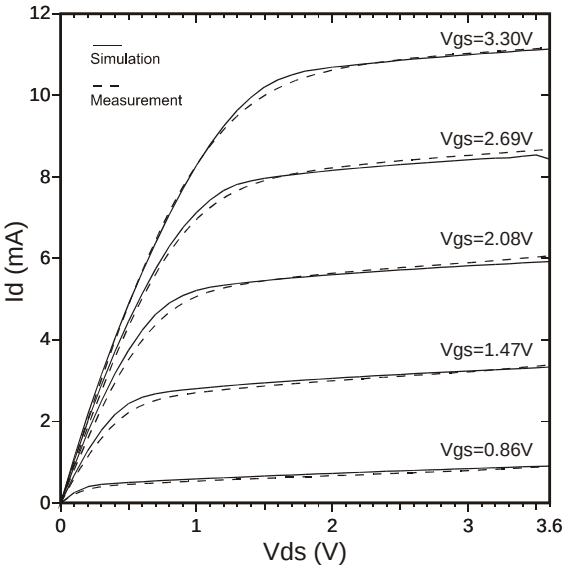

Fig. 3 Output characteristics n-MOSFET

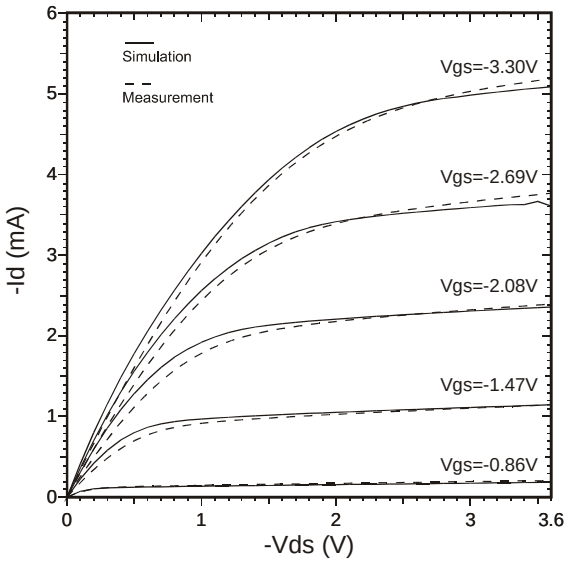

Fig. 4 Output characteristics p-MOSFET

By using precise doping profiles and a suitable model for the poly silicon gates a good agreement with measured values could be reached. The threshold voltages are 0.5 V and –0.5 V for the n- and p-channel transistor, respectively. The transconductance of the n-MOSFET at Vgs = 2 V, Vds = 1.3 V amounts g_m = 4 mS whereas g_m = 1.7 mS is obtained for the p-MOSFET at Vgs = -2 V, Vds = -1.3 V.

Fig. 5 and **Fig. 6** show the small-signal gains MSG/MAG and h_{21} at different working points.

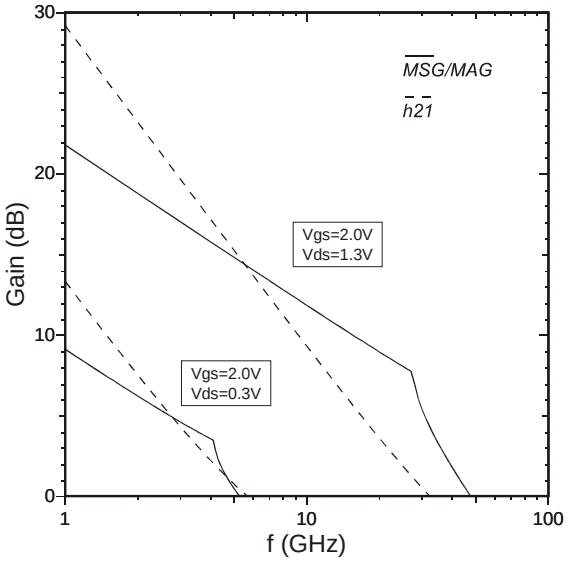

Fig. 5 Small-signal gains n-MOSFET

A maximum oscillation frequency f_{max} = 47 GHz and a transit frequency f_T = 32 GHz was achieved in the saturation region. These values correspond to

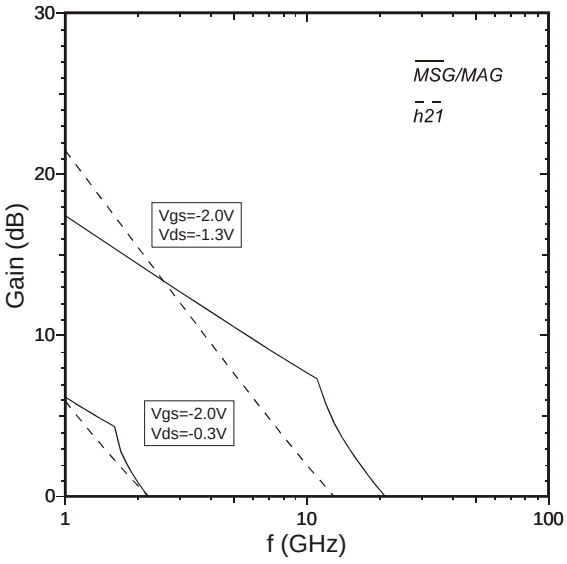

Fig. 6 Small-signal gains p-MOSFET

experimental results. For the p-MOSFET f_{max} = 21 GHz and f_T = 13 GHz are obtained at the same working point.

4 Structure Variations

For the determination of the influence of tolerances in the technology process and for the device optimization different structure parameters are varied. The effect of gate length variation in the range of (350 ± 50) nm on output characteristics is represented in **Fig. 7** and **Fig. 8**.

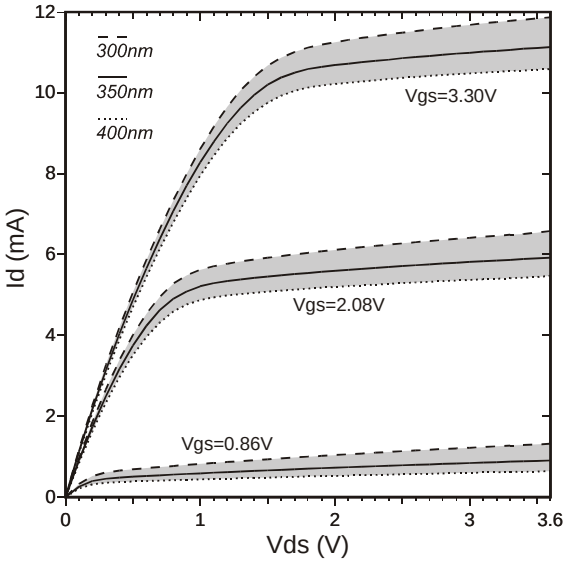

Fig. 7 Output characteristics n-MOSFET for different gate lengths

As expected smaller gate lengths result in higher drain currents as well as in increasing transconductances. Thus the RF behavior is modified as plotted in **Fig. 8** and **Fig. 9** for the n- and p-MOSFET, respectively.

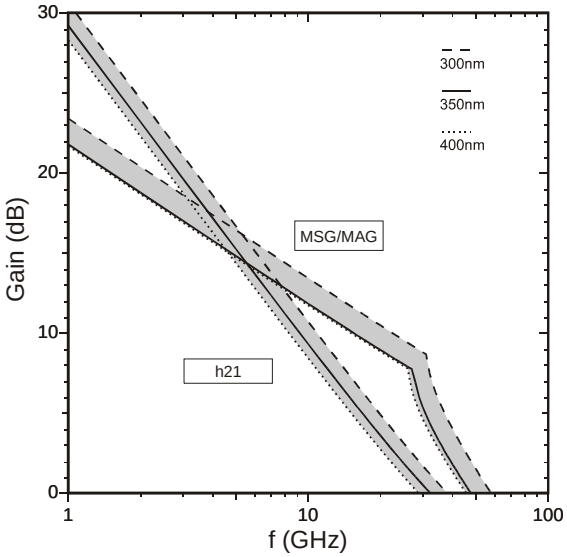

Fig. 8 Small-signal gains n-MOSFET for different gate lengths

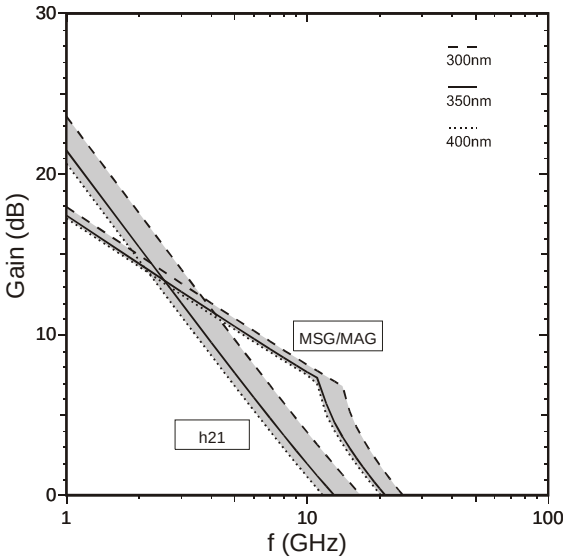

Fig. 9 Small-signal gains p-MOSFET for different gate lengths

The corresponding cut-off frequencies for the different gate lengths are summarized in **Tab. 1** for n- and p-channel transistors. The increase of the cut-off frequencies at gate length shortening is about five times greater in comparison with the decrease of the cut-off frequencies at larger gates. A similar behavior is obtained at the dependence of the gains on the different gate lengths.

	n-MOSFET		p-MOSFET	
Lg (nm)	f_T (GHz)	f_{max} (GHz)	f_T (GHz)	f_{max} (GHz)
300	38	58	17	25
350	32	48	13	21
400	29	46	11	20

Tab. 1 Cut-off frequencies for different gate lengths

As a further example of parameter variation the influence of the lightly doped drain regions (LDD) is represented.

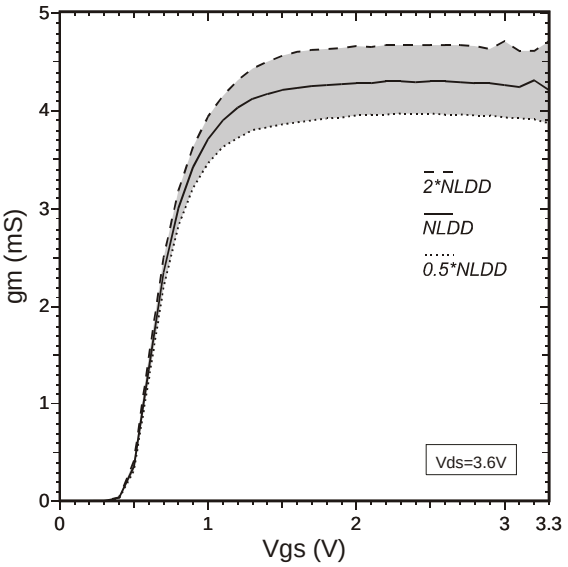

Fig. 10 Transconductance versus gate-source-voltage at different LDD doping levels (n-MOSFET)

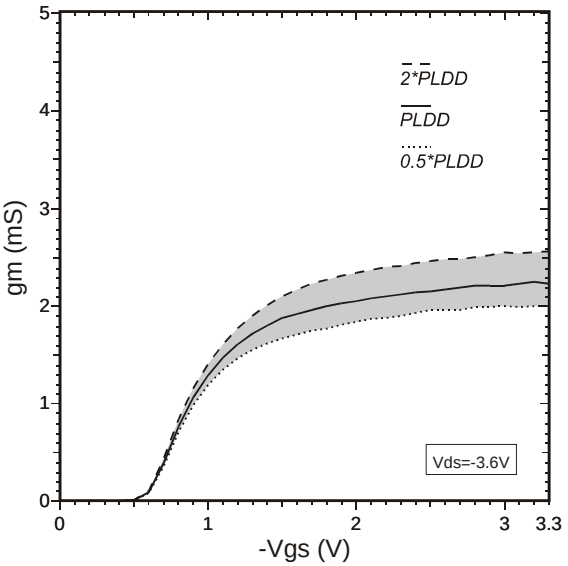

Fig. 11 Transconductance versus gate-source-voltage at different LDD doping levels (p-MOSFET)

Fig. 10 and **Fig. 11** show the transconductance of n- and p-MOSFET, if the maximum doping N_{LDD} (n-channel) and P_{LDD} (p-channel) of the LDD-regions is doubled and halved, respectively. The variation of LDD-doping results in a change of drain saturation current in a range of ± 10 % of the basic values. In a comparable range the transconductances are modified, increasing tranconductances are caused by larger doping levels.
The RF behavior is represented in **Fig. 12** and **Fig. 13**. At the n-channel transistor the gains and consequently the cut-off frequencies are changed only slightly whereas the p-channel transistor shows obvious dependence on LDD-doping. This behavior results from larger variation of the gate-drain-capacity due to a displacement of the p-LDD-region. Further variations show convenient RF-behavior at asymmetric source/drain dopings.

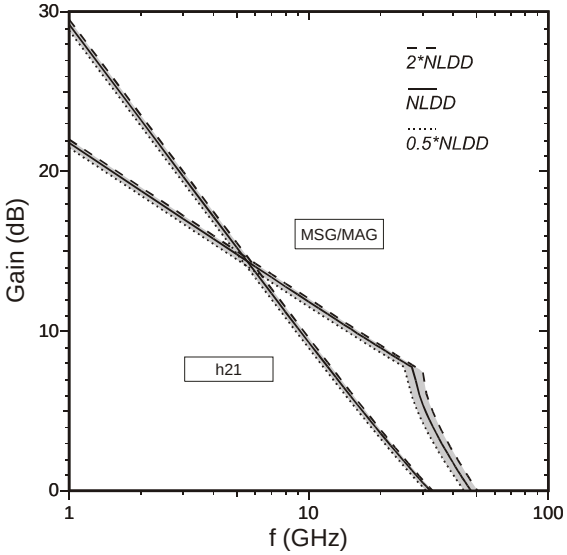

Fig. 12 Small-signal gains at different LDD doping levels (n-MOSFET)

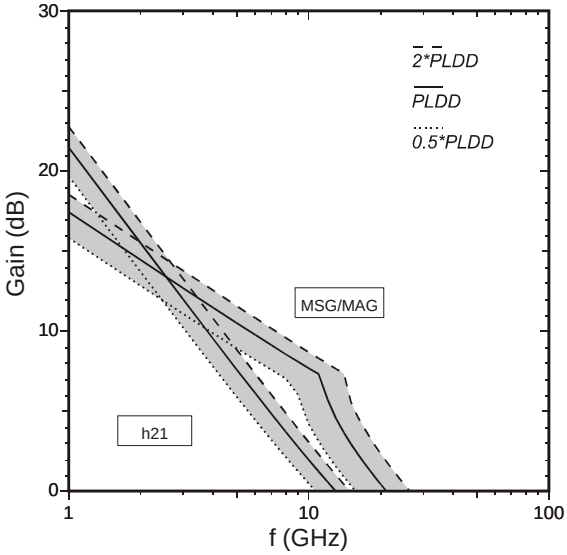

Fig. 13 Small-signal gains at different LDD doping levels (p-MOSFET)

5 Conclusions

Numerical simulation of n- and p-channel transistors of a CMOS technology have been carried out to find out the RF behavior of these structures. The calculated results agree well with experimental values. The variations of different structure parameters show the influence of technological deviations and give hints for structure optimizations.

6 Literature

[1] W. Klix, R. Dittmann, R. Stenzel: Three-dimensional simulation of semiconductor devices. Lecture Notes in Computer Science 796, Springer-Verlag, 1994, pp. 99-104

[2] R. Stenzel, C. Pigorsch, W. Klix: Simulation von Nanobauelementen. PTB-Bericht F-31, Physikalisch-Technische Bundesanstalt Braunschweig, 1998, S. 56-65

[3] R. Stenzel, W. Klix: SIMBA – ein universeller 3D-Bauelementesimulator. Berichte und Informationen, HTW-Dresden 2/1999,1/2000, S. 51 - 56