NUMERICAL SIMULATION OF SMALL SILICON PARTIALLY INSULATED MOSFETS

Wilfried KLIX, Roland STENZEL, Tom HERRMANN
Department of Electrical Engineering
University of Applied Sciences Dresden
Friedrich-List-Platz 1, D-01069 Dresden
Mail: klix@et.htw-dresden.de

1. Introduction

The scaling of conventional MOS bulk transistors seems to be difficult due to short channel effects. Especially the threshold voltage V_{th} is difficult to control and drops down rapidly at short gate lengths. SOI technologies have been developed to overcome the difficulties, but floating body effects, increasing leakage currents and in general, a lower V_{th} appears. Therefore the partially insulated FET (Pi-FET) with oxide under source and drain seems to be a candidate for scaling down the gate length into the submicron area and combine the benefits of conventional and SOI MOSFETs [1],[2],[3].

2. Simulation model

For the simulations of the several MOS transistors we have used our 2D/3D simulation program SIMBA whereas only the conventional drift-diffusion-model was used. The basic equations Poisson equation, continuity equations the transport equations are solved numerically by using a box method for discretization [4].

For the simulation of the leakage currents and kink-phenomena the avalanche generation and band-to-band tunnel generation model was included [4]

$$G_{AV} = \alpha_p \cdot \left|\mathbf{J}_p\right| + \alpha_n \cdot \left|\mathbf{J}_n\right|, \qquad G_{BB} = A_{BB} \frac{E^2}{\sqrt{W_g}} \cdot \exp\left(- B_{BB} \frac{W_g^{3/2}}{E} \right) .$$

3. Results

Several simulations have been carried out to compare conventional bulk FET's, SOI- and partially insulated FET's. In Figure 1 the doping profile of these structures is illustrated. The gate length is about 40 nm. In Figure 2 the simulated output characteristics are shown. The SOI-FET has a kink-effect due to avalanche generation, whereas the partially insulated FET does not have such behaviour. The calculated transfer characteristics are shown in Figure 3. Further more simulations have been carried out to determine the threshold voltage V_{th} for all structures as a function of the gate length and the electrical behaviour of the Pi-FET at different gaps between the oxide regions.

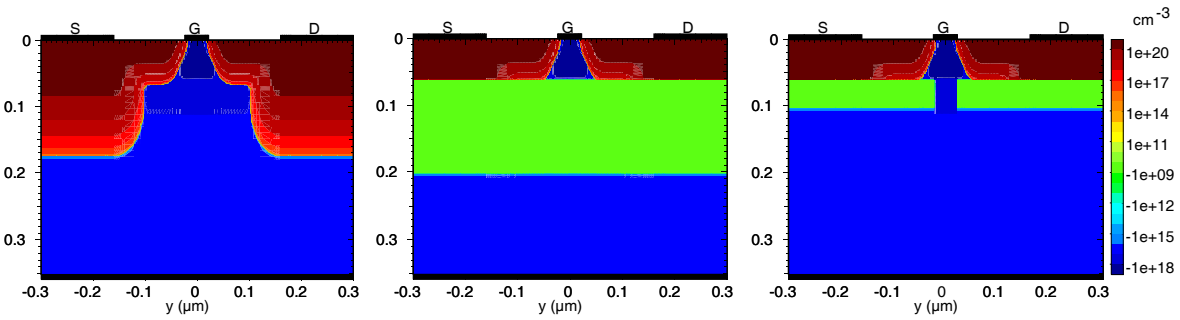
References

[1] *C. L. Chen, S. J. Spector et al. :* High-Performance Fully-Depleted SOI RF CMOS, IEEE Electron Device Letters, Vol. 23, No. 1, Jan. 2002, pp. 52-54.

[2] *K. H. Yeo, Ch. W. Oh et al.:* A Partially Insulated Field-Effect Transistor (PiFET) as a Candidate for Scaled Transistors, IEEE Electron Device Letters, Vol. 25, No. 6, June 2004, pp. 387-389.

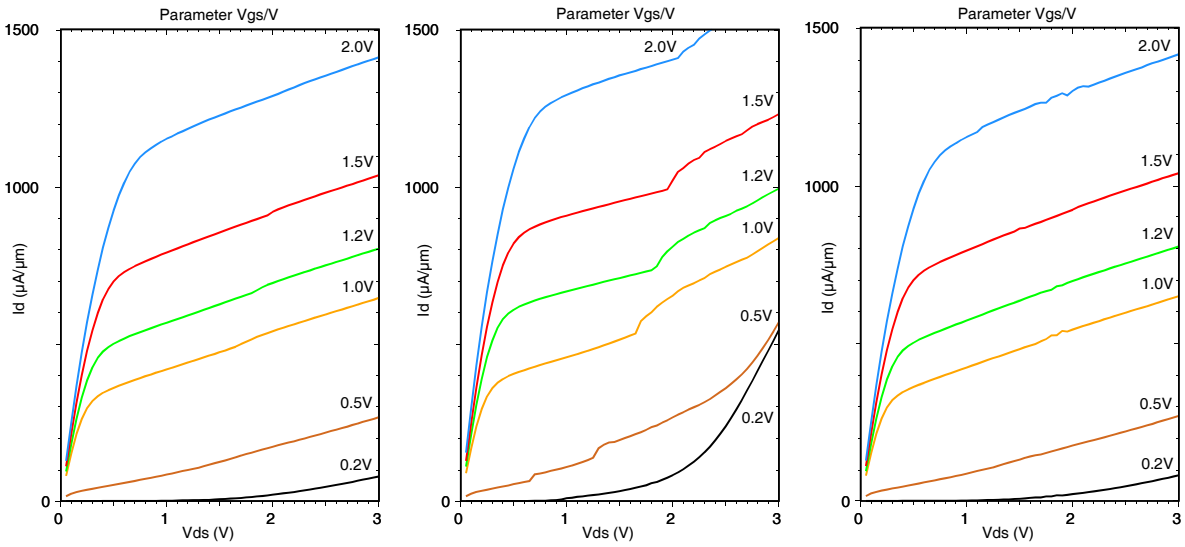
[3] *Ch. W. Oh, K. H. Yeo, et al.:* Electrical Characterization of Partially Insulated MOSFET's with Buried Insulators under Source/Drain Regions, IEEE Trans. on ED 2004, pp. 233-236.

[4] W. *Klix, R. Stenzel:* Program System SIMBA, Models and Solution Methods. http://www.htw-dresden.de/~klix/simba/welcome.html



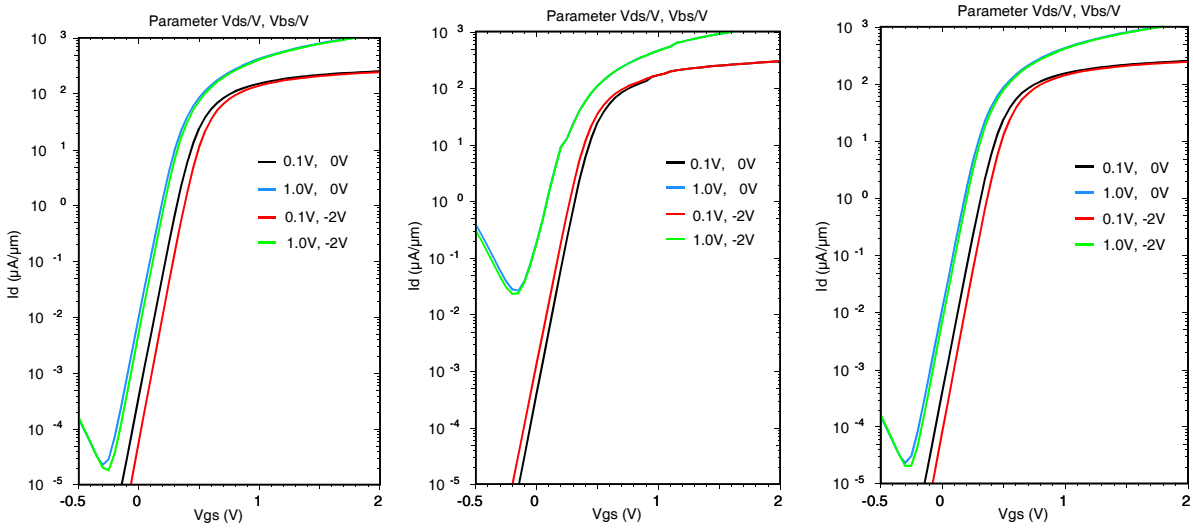
a) Bulk MOSFET b) SOI-MOSFET c) Pi-FET

Fig. 1: Doping profiles



a) Bulk MOSFET b) SOI-MOSFET c) Pi-FET

Fig. 2: Simulated output characteristics



a) Bulk MOSFET b) SOI-MOSFET c) Pi-FET

Fig. 3: Simulated transfer characteristics