Optimization of High Performance Nano Scaled SOI-MOSFETs by Process and Device Simulation

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Abstract

This paper will give an overview about the simulation of current high performance SOI-MOSFETs in order to optimize the manufacturing process. The results for varied process parameters of halo implantations and laser annealing are shown.

1. Introduction

The international technology roadmap for semiconductors (ITRS) 2004 predicted a gate length of 32 nm for the year 2005 and a further reduction to 20 nm till the year 2009 for high performance transistors. These dimensions could not only be achieved with classical scaling. In the past several technologies were introduced to further reduce the transistor size. One example is the so called super-halo implantation [1], which decrease the short channel effect. New technologies like non-melt laser annealing (LA) for high activated and less diffusing doping profiles are under development [2] and might replace the rapid thermal annealing (RTA).

The process and device simulations of these technologies are in the following presented in order to show the transistor optimization by means of simulation tools.

2. Process and device simulation

Process simulation tools allow the complex and fast modelling of almost every process step. The mathematic models have to be calibrated with measurements of fabricated test structures. Thereafter a simplified process flow has to be created in order to get the basic transistor (Fig. 1). This process flow could now be varied with the different approaches for optimization.

The device simulation tools basically solve the poisson equation, the continuity equations and the transport equations. This set of equations is called the drift diffusion model. It is the simplest variant, which underestimates the saturation current in short channel devices. A

more complex model is the hydrodynamic transport model, which takes into account the carrier temperature. Therefore more accurate carrier velocities are predicted. Furthermore several mobility and recombination models could be used. SOI-MOSFETs are sensitive to minority carrier generation which reduces the body potential and leads to kinks (Fig. 2) in the characteristic curves or dynamic threshold voltage behaviour. Most important is the generation through tunneling mechanisms and impact ionization. Due to the thick buried oxide, the heat flux from the silicon film to the substrate is inhibited. A higher lattice temperature leads to lower carrier mobility in the silicon film and therefore to lower saturation currents. Anymore the small dimension cause quantum effects in the inversion channel. A fast and accurate way to consider quantization effects is the quantum drift diffusion model or the density gradient model. The calculated quantum potential modifies the band edge, which results in a continuous carrier distribution.

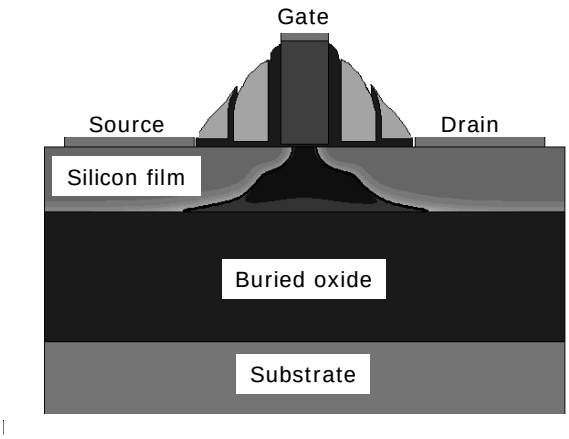

Figure 1: Structure of the basic transistor

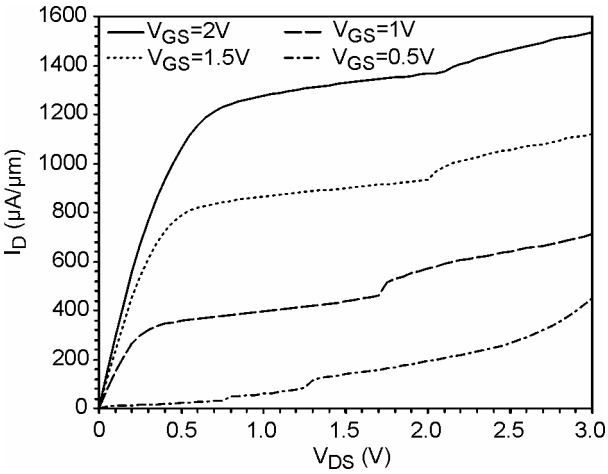

Figure 2: Output characteristics with the impact ionization model

3. Transistor optimization

Halo implantations are inserted to increase the substrate doping around the extension areas. The extension depletion regions get smaller and the gate may control more of the channel charge. Medium energy halo implantations are situated in the middle of the silicon film and overlap each other in nano scaled transistors. The lateral channel profile is almost uniform and thereby these halo implantations are less effective.

A PD-SOI-n-MOSFET with halo implantation energies ranging from 9 keV down to 2 keV and a gate length of 55 nm has been simulated. The lateral edge of the boron maximum moved from the middle of the silicon film to the surface and the gate edge. The lateral channel and the vertical extension doping profile shows a higher p-type doping concentration near the pn-

junction of the extension regions due to the smaller width of low energy implantations and the higher dopant dose, which is required to match the threshold voltage. Thus the extension depletion regions become smaller and therefore less influence on the channel charge occurs. The threshold voltage is less affected by the gate length reduction (Fig. 3). The universal curve (Fig. 4) shows no degradation for decreased halo implantation energies till 3 keV at matched threshold voltage and overlap capacitance.

A decreasing doping concentration in the well near the silicon/buried oxide interface led to a leakage path at the interface in combination with an amount of $4 \cdot 10^{10}\,cm^{-2}$ fixed oxide charges in the vicinity of the buried oxide as can be seen for the 3 keV halo implantation energy in Fig. 4.

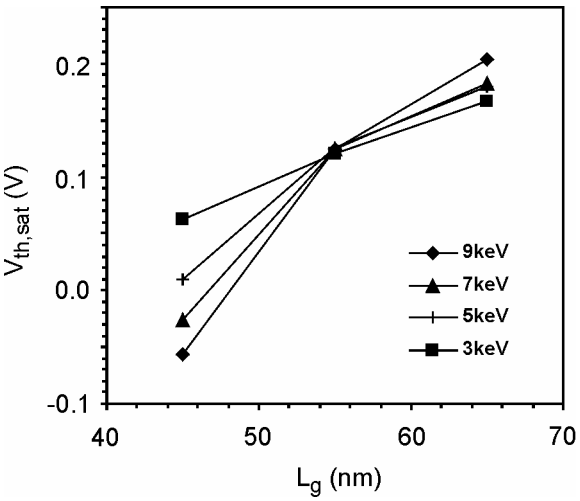

Figure 3: Short channel behavior for different halo implantation energies

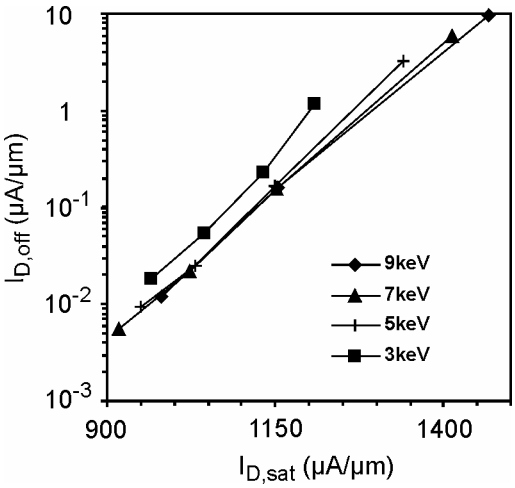

Figure 4: Universal curve for different halo implantation energies

The halo implantation dose has been raised exponential to achieve the same threshold voltage while decreasing the halo implantation energy. This leads to counter doping of the extension and source/drain areas. For halo implantation energies below 3 keV a surface p-region is build instead of the upper source and drain areas.

Dopant annealing methods with short times and high temperatures like non-melt LA are of increasing interest for nano scaled MOSFETs. The weak diffusion and high dopant activation promise better scalability and higher transistor performance.

Starting from the standard manufacturing process, the diffusion time and temperature was set to 1 µs and 1350 °C. The result is a non-diffusing dopant profile with an amount of active dopant near the solid solubility limit. The thickness of the offset spacer, which is necessary to control the overlap of the extension regions, had to be reduced to 2 nm without reaching the

overlap of the RTA device. The resulting channel length is therefore about 60 % longer. Under these conditions the device performance was significantly declined. A 3 times higher threshold voltage and a 10 % degraded universal curve could be observed.

A commonly used method to adjust the threshold voltage is the reduction of the halo implantation dose. Applied to the transistors with non-diffusing doping profile, a 1/5 lower dose could be used to achieve the same threshold voltage with a better short channel behavior, which is shown in Fig. 5. Therefore the amount of dopant in the channel region is reduced and less carrier scattering takes place. The carrier mobility raised and the universal curve is about 27 % improved (Fig. 6). If half the halo implantation dose of the RTA device is used, the gate length could be reduced to 25 nm with the same threshold voltage (arrow in Fig. 5), a comparable short channel behaviour and a slightly improved universal curve.

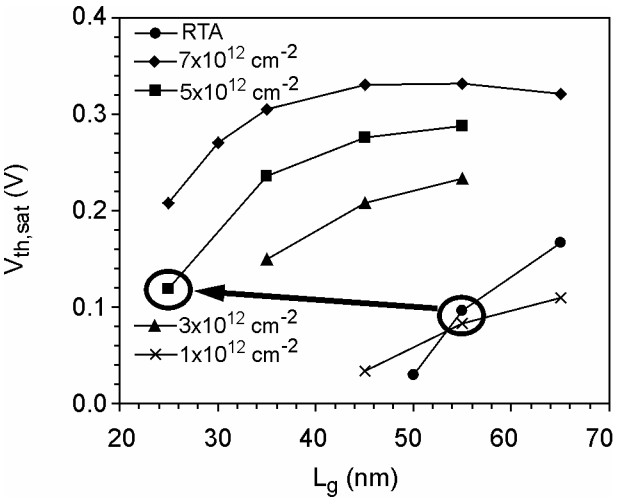

Figure 5: Short channel behaviour for various halo implantation doses

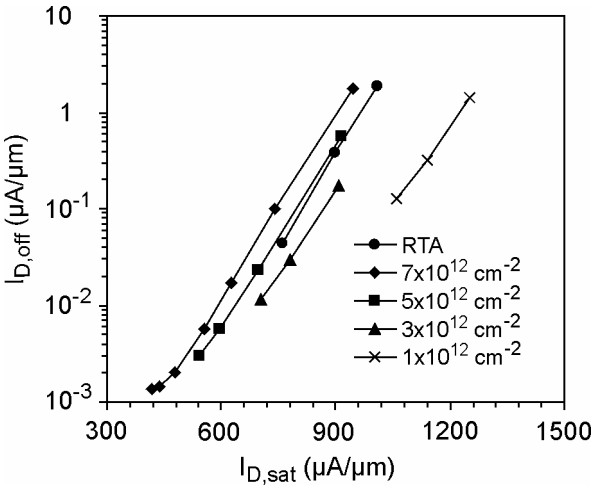

Figure 6: Universal curve for various halo implantation doses

4. Results

A reduction of the halo implantation energy decreased the short channel effect with only few degradation of the universal curve. It had to be done carefully because of a possible leakage path at the buried oxide. The non-diffusing doping profiles have a high potential to increase the transistor performance in terms of short channel behavior, universal curve.

5. References

[1] Taur, Y., Wann, C.H. and Frank, J.D.: 25nm CMOS Design Considerations. IEDM Tech. Dig. 1998, 789 - 792

[2] Shima, A., Wang, Y., Talwar, S. and Hiraiwa, A.: Ultra-shallow junction formation by non-melt laser spike anneal. Symp. VLSI Tech. Dig. 2004, 174 – 175