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# Power handling limits and degradation of large area AlGaIn/GaN RF-HEMTs

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## Abstract

We investigate the influence of the device geometry of large scale RF power AlGaIn/GaN-HEMTs on the RF output power density. Multifinger-RF-HEMTs with different device geometries were fabricated on comparable epilayers grown on both sapphire and SiC substrates. Thermal impedances of the different FETs were measured and simulated. We discuss the correlation between the thermal device impedance and the RF output power, measured at 2 GHz. Degradation phenomena under high temperature and high current conditions are reported. As a result, we show that the thermal device impedance can be used as a design rule for the optimization of AlGaIn/GaN-RF-HEMTs.

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## 1. Introduction

System designers of high-power RF-modules require RF-devices with high absolute power output and high operating voltage. In the past this has invoked a great interest in large-scale AlGaIn/GaN high electron mobility transistors (HEMTs). However, increasing device output power is associated with an increasing power dissipation of the devices. Although small AlGaIn/GaN HEMTs grown on SiC substrate have already demonstrated high power densities of 10.7 W/mm at 10 GHz [1], large devices cannot attain these power densities. Therefore, it is of major importance to effectively remove the dissipated heat from the device. Several papers have already discussed the thermal advantages of SiC compared to sapphire as substrate material [3–5]. In this paper we will focus on the impact of the device geometry on the thermal properties, the maximum output power at RF-frequencies and their degradation.

## 2. Device fabrication

Four-finger-FETs with comb shaped gate structures were fabricated from equivalent epilayers on sapphire and SiC substrates. Details of the fabrication process can be found in [2]. The sheet carrier concentration and the mobility is  $8 \times 10^{12} \text{ cm}^{-3}$  and  $1000 \text{ cm}^2/\text{Vs}$  for the epilayer on SiC, respectively  $1 \times 10^{13} \text{ cm}^{-3}$  and  $1450 \text{ cm}^2/\text{Vs}$  for the epilayer on sapphire. The Al-content is 20%. One-finger-FETs on both wafers exhibit a maximum drain current of 1000 mA/mm and a maximum transconductance of 270 mS/mm at a gate length of 0.3  $\mu\text{m}$ . The four-finger-FETs are different in gate pitch (i.e. spacing between adjacent gates) and mesawidth.

## 3. Thermal characterization

To compare the thermal properties of the different device structures, a method similar to [5] is used to determine the thermal device impedances  $\vartheta = \partial T / \partial P$ . In Fig. 1a a strong dependence of  $\vartheta$  on the device geometry is observed. The thermal impedance increases with increasing mesawidth and decreasing gate pitch. Increasing the mesawidth enlarges the device area linearly. A small

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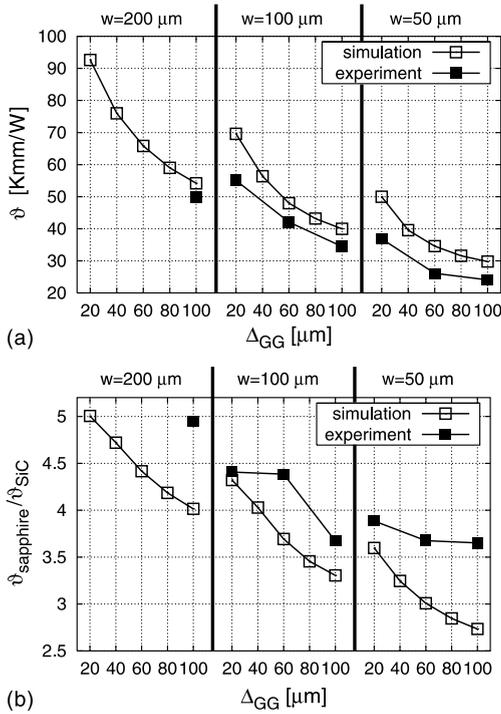


Fig. 1. (a) Thermal device impedances of four-finger-FETs on sapphire with different gate pitches  $\Delta_{GG}$  and different mesa-widths  $w$ ; simulation performed with 3D simulator SIMBA; (b) ratio of thermal device impedances of devices on sapphire and SiC substrate.

device can be regarded as a point shaped heat source where the heat is removed with radial symmetry into the heatsink halfplane (substrate and GaN buffer). However, for large devices the contribution of the boundary to the total heat removal is reduced. The heat is conducted into the substrate primarily perpendicular to the surface resulting in a higher thermal device impedance. In the same way a decrease in gate pitch increases  $\vartheta$ . A small gate pitch reduces the lateral heat removal from the channel region into the contact region and increases the thermal coupling between adjacent gates.

The experimental results are compared with simulated values for  $\vartheta$ . The 3D-simulator SIMBA is used to incorporate the effect of the airbridge metalization. The different thermal conductivities of the substrate (thickness  $300 \mu\text{m}$ ,  $\lambda_{\text{sapphire}} = 50 \text{ W/K m}$ ,  $\lambda_{\text{SiC}} = 500 \text{ W/K m}$ ), the GaN buffer (thickness  $3 \mu\text{m}$ ,  $\lambda_{\text{GaN}} = 130 \text{ W/K m}$ ) and the metalization (thickness  $3 \mu\text{m}$ ,  $\lambda_{\text{Au}} = 300 \text{ W/K m}$ ) are taken into account. The substrate boundary is kept at  $300 \text{ K}$  and the heat flow equation  $\nabla^2 T = -H/\lambda$  is solved. It is assumed that the heat is generated homogeneously in a  $20 \text{ nm}$  thick channel between the source and drain contact of  $2.5 \mu\text{m}$  spacing. To determine the thermal device impedance from simulation the maximum channel temperature is used. However, the mea-

surement procedure inherently uses a mean channel temperature to determine  $\vartheta$ . Consequently, the simulated values are systematically higher than the measured ones. Taking this into account, the simulated and measured values are in good agreement. Therefore, our simulation can be applied to judge a device geometry with respect to its thermal properties.

Furthermore, the influence of the metalization and the substrate thickness on  $\vartheta$  were investigated with SIMBA. Omitting the gold metalization it is found for the first FET in Fig. 1a ( $w = 200 \mu\text{m}$ ,  $\Delta_{GG} = 20 \mu\text{m}$ , sapphire substrate) that the thermal device impedance increases by  $16 \text{ K mm/W}$ . This shows that the gold metalization can effectively spread heat from the channel region into the contact region. An  $80 \mu\text{m}$  thick substrate compared to  $300 \mu\text{m}$  reduces  $\vartheta$  of the same FET by  $22 \text{ K mm/W}$ . Therefore, substrates of large scale devices should be thinned.

In Fig. 1b the ratio of the thermal device impedances of FETs on sapphire and SiC substrates is shown. The ratio is far below the value of 10, determined from the bulk thermal conductivities of sapphire and SiC. For devices with small mesowidths and large gate pitches, the heat spreading of the GaN buffer and the Au metalization is significant. Hence, the thermal advantages of SiC substrates are well reduced. Only for very large devices with small gate pitches and large mesowidths the influence of the substrate becomes dominant. This result is not in contradiction with [5], where the ratio of the thermal device impedances was  $>10$ . In [5] no RF-devices (large source to drain spacing), no Au metalization and a thinner GaN buffer were used. This reduces the influence of the discussed heat spreading effects significantly.

#### 4. RF power density and degradation

To demonstrate the importance of the thermal device impedance for the maximization of the RF output power, the measured power density at  $2 \text{ GHz}$  is plotted over  $\vartheta$  from simulation (Fig. 2). In the range of  $10.5 \text{ K mm/W} \leq \vartheta \leq 14.2 \text{ K mm/W}$ , the RF output power is reduced by a factor of  $\approx 2$ . Within the experimental error a linear relationship can be assumed. This shows that the thermal device impedance can be used as a design rule for the optimization of large scale RF power AlGaIn/GaN HEMTs.

An important issue for RF-power-HEMTs is degradation. To test the reliability of the different devices, SiC HEMTs are stressed at  $V_{\text{ds}} = 20 \text{ V}$  with a dc power dissipation of  $15 \text{ W/mm}$ . Assuming a PAE of 40% under RF-conditions, an RF-output power of  $10 \text{ W/mm}$  would generate the indicated power dissipation. After 5 min the drain current  $I_{\text{d}}$  is measured and compared to its value at the beginning of the stress procedure (see Fig. 3). Within

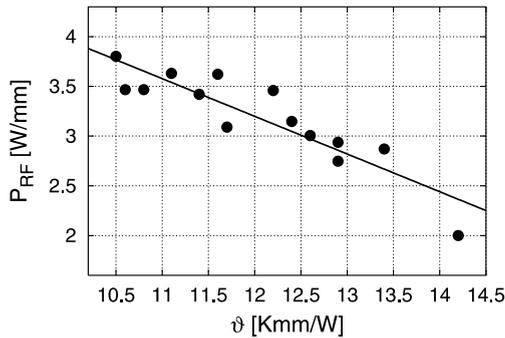


Fig. 2. Devices on SiC substrate: measured RF output power at 2 GHz plotted over the simulated thermal device impedances; line fitted to the experimental data.

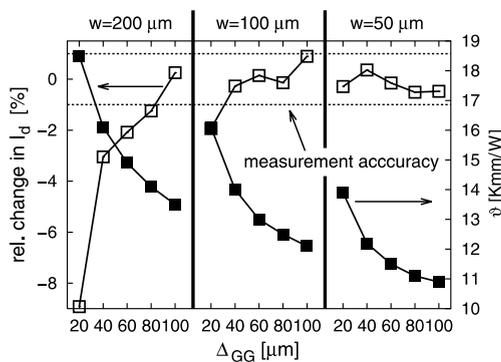


Fig. 3. Devices on SiC substrate: device degradation after 1 min biasing at  $V_{ds} = 20$  V and  $P_{dc} = 15$  W/mm.

the experimental error of 1% for  $I_d$  all devices with  $\vartheta > 14$  K mm/W degrade. The devices on sapphire are stressed at 5 W/mm and degrade if  $\vartheta > 45$  K mm/W (not shown).

During the stress procedure, the maximum temperature of the SiC devices is  $\approx 300$  °C. This temperature is too low to invoke degradation of the semiconductor [6]. However, the temperature in conjunction with the high current densities is high enough to cause electromigration in the metalization [7]. The electromigration in the source fingers can be seen in SEM pictures. Electrically, the degradation is observed in the source resistance  $R_s$ .

For the first FET in Fig. 3,  $R_s$  is increased from 1 to 1.4  $\Omega$  mm during the stress procedure described above.

In conclusion we have shown that a reduction of the thermal device impedance of AlGaIn/GaN RF-power-HEMTs increases the output power density. Therefore, the thermal device impedance  $\vartheta$  is a design rule for maximization of the RF output power.  $\vartheta$  can be reduced by increasing the gate pitch and decreasing the mesa-width. A thick Au metalization and a thin substrate further reduce the thermal device impedance due to heat spreading effects. The heat spreading is responsible for the low ratio  $\vartheta_{\text{sapphire}}/\vartheta_{\text{SiC}}$  of 3–5 for typical device layouts. For  $\vartheta > 14$  K mm/W and a power dissipation of 15 W/mm, the devices suffer from pronounced degradation due to electromigration in the Au metalization. This indicates, that low thermal impedances and metalizations with large cross-section areas are required to provide reliable high-power operation.

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