Scalability of Advanced Partially Depleted n-MOSFET Devices on Biaxial Strained SOI Substrates

S. Flachowsky[1], J. Höntschel[2], A. Wei[2], R. Illgen[1], P. Hermann[3], T. Herrmann[1], W. Klix[1], R. Stenzel[1], A. Ramirez[2], M. Horstmann[2], N. Kernevez[4], I. Cayrefourcq[4], F. Metral[4], M. Kennard[4], and E. Guiot[4]

[1] Department of Electrical Engineering, University of Applied Sciences Dresden, Friedrich-List-Platz 1, D-01069 Dresden, Germany
[2] AMD Fab 36 LLC &Co. KG, Wilschdorfer Landstraße 101, D-01109 Dresden, Germany
[3] Fraunhofer Center für Nanoelektronische Technologien, Königsbrücker Straße 180, D-01099 Dresden, Germany
[4] SOITEC, Parc technologique des Fontaines, Bernin 38926 Crolles Cedex, France

Email: stefan.flachowsky@et.htw-dresden.de; Phone: +49 351 4623428

Biaxial tensile strained substrates offer strong electron mobility enhancements resulting in large drive current gains. For short channel n-MOSFETs, however, these improvements diminish. Root causes for this performance degradation are investigated through experiments and simulations. Elastic stress relaxation arising from shallow trench isolation (STI) is found to be negligible for current state-of-the-art transistors. On the other hand, parasitic source/drain resistance seems to be responsible for the limitation of drain current gains in deeply scaled devices. This effect is even further aggravated by an increased parasitic source/drain resistance in sSOI devices compared to standard SOI.

1. Introduction

Biaxial tensile strain in silicon is an effective way to enhance the electron mobility and thus the drive current of n-MOSFET devices. Strained silicon on insulator substrates (sSOI) introduce high tensile and uniform strain levels directly into the channel region [1] combined with the advantages of SOI substrates (reduced parasitic capacitances and a higher integration density). Electron mobility enhancements up to 125 % have been reported for long-channel devices [2], with concomitant drive current increase of up to 80 % on long channel n-MOSFETs. However, several authors have reported a dramatic reduction in biaxial strained n-MOSFET performance enhancement as the channel length decreases [1],[3]. There can be several explanations proposed for this behavior [4],[5]: a) approaching the saturation velocity due to higher electrical fields in scaled devices b) higher stress relaxation in smaller structures caused by closer free surfaces from STI formation c) increasing parasitic source/drain resistance ($R_{S/D}$) influence in short channel devices masking the strain-induced mobility enhancement or d) degraded coulomb mobility in the channel region due to higher channel doping.

This study employs experimental work combined with process and device simulations to separate the root causes for this unfavorable scaling behavior. Measurements show that for short channels, the strain-enhanced mobility benefit of sSOI is preserved, which would contradict theories related to strain relaxation. An increased $R_{S/D}$ in sSOI compared to conventional SOI devices has thus been identified and verified in this study as the major mechanism.

2. Device Fabrication

n-MOSFETs with gate lengths down to 40 nm (Fig. 1) were fabricated on both SOI and sSOI wafers using SiON as gate dielectric and polysilicon as gate material [6] in a leading-edge 65nm SOI technology with contacted poly pitch of 270 nm. The biaxial stress in the 60 nm thick sSOI layer resulting from the relaxed $Si_{0.8}Ge_{0.2}$ buffer layer was measured by Raman spectroscopy to be ~1.3 GPa. To account for the enhanced diffusion of n-type dopants in sSOI substrates the ion implantation doses of the extension regions was reduced by roughly 25 %. The investigated devices were targeted for identical overlap-capacitance and DIBL. No other intentional stress sources like strained overlayer films or stress memorization techniques were implemented into the devices to avoid interactions of the different stressors, especially for varying device dimensions.

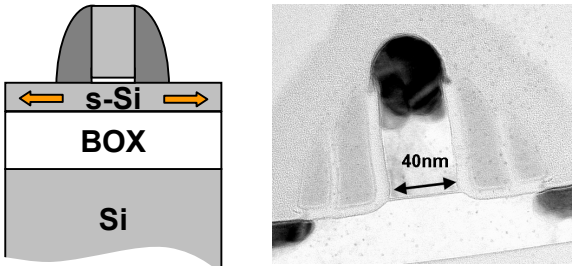

Fig. 1 Schematic transistor layout of a sSOI device and TEM cross section of a 40 nm sSOI n-MOSFET [3].

3. Process & Device Modeling

Using SYNOPSYS Sentaurus TCAD software, 2-D finite element simulations are performed to analyze the stress distribution in various structures. The simulator uses the plane-strain condition, in which the out-of-plane elongation is set to zero, which is a valid assumption for large width transistors. Silicon was treated as an anisotropic elastic material.

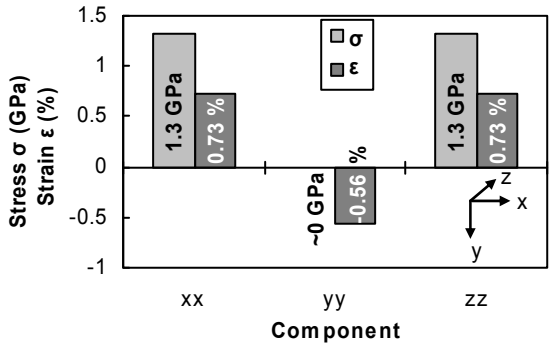

Fig. 2 Simulated strain and stress components in an infinite sSOI layer. Tensile stresses/strains are positive, while compressive stresses/strains have a negative sign.

The calculated strain and stress components in this biaxial tensile strained Si layer are shown in Fig. 2. The in-plane strain $\varepsilon_{xx}=\varepsilon_{zz}$ is 0.73 % for an underlying $Si_{0.8}Ge_{0.2}$-layer and the corresponding out-of-plane strain ε_{yy} is -0.56 %.

The vertical stress distribution through the sSOI-wafer obtained from Raman spectroscopy measurements is shown in Fig. 3. The higher tensile stress at the silicon surface compared to the bottom near the buried oxide layer can be attributed to the Smart Cut™ fabrication process [7]. In this process the strained Si layer is bonded upside down on the oxide layer. Since only the stress in the top most few nm, where the transistor channel will be situated, is of interest, a uniform stress distribution of 1.3 GPa within the Si layer was assumed in the simulation.

The process and device simulation models for the analysis of the electrical transistor behavior were calibrated using measured SIMS profiles, TEM cross sections and transfer and output characteristics of a state-of-the-art SOI transistor [6].

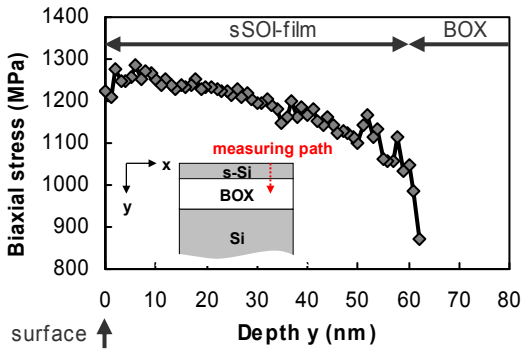

Fig. 3 Raman spectroscopy measurement of the stress distribution along the sSOI film thickness.

4. Results and Discussion

4.1 Stress Simulation Results

Free surface strain relaxation can occur during shallow trench isolation (STI) formation which greatly influences the strain distribution of sSOI layers and thus the potential transistor channel. As can be seen from Fig. 4, the originally homogenous strain in the sSOI layer becomes strongly disturbed after the island formation. Near the STI corners a strong elastic relaxation occurs which is more serious at the silicon surface because the sSOI film is constrained only at the bottom to the underlying oxide layer. For smaller silicon island lengths the relaxation extends significantly throughout the entire film.

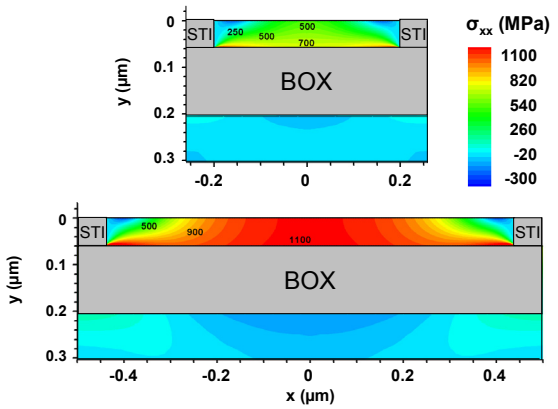

Fig. 4 Simulated stress distribution in STI structured sSOI islands for different lengths (0.4 µm, top; and 0.9 µm, bottom).

This is investigated in more detail in Fig. 5 which shows a cut along the top surface in a depth of 2 nm for various island sizes. For long regions only the silicon edges suffer from relaxation whereas for regions shorter 1 µm also the maximum stress value in the center reduces.

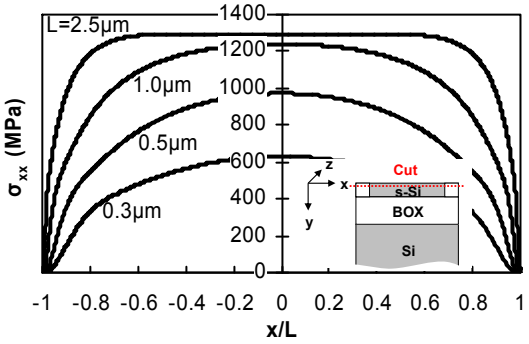

Fig. 5 Stress along the normalized length taken 2 nm below the surface for different sSOI island lengths.

Fig. 6 illustrates the relaxation behavior for different silicon film heights H and film lengths L, where the stress in the center of the structure was taken (see inset of Fig. 6). As expected, higher films experience more stress loss from relaxation, as do shorter films.

A more extensive study of various film heights and film lengths reveals that there is only a dependency on the geometrical aspect ratio of these two parameters and not of the absolute values themselves.

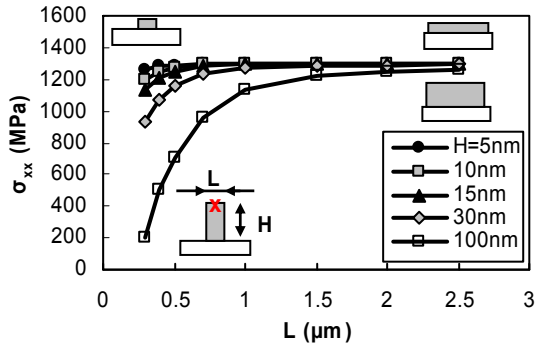

Fig. 6 Stress in the structure center (x) for various film heights and lengths of the sSOI islands.

Fig. 7 shows the horizontal stress in the center of a structure σ_{xx} normalized to the maximum stress $\sigma_{xx,\infty}$ in an unstructured sSOI layer for a variety of structure aspect ratios. For very thin and long silicon layers there is negligible stress relaxation but for longer and thicker structures the relaxation increases. Interestingly, between $0.2 < H/L < 2.0$ a region with negative $\sigma_{xx}/\sigma_{xx,\infty}$ exists, which has to be interpreted as a compressive stressed area in an otherwise tensile strained Si layer.

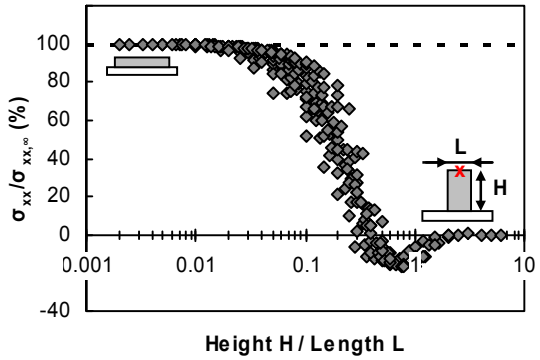

Fig. 7 Simulated normalized stress in the structure center for various geometrical aspect ratios of the sSOI island.

To illustrate this effect, the stress contour maps are plotted in Fig. 8 for four different aspect ratios. There is always a compressive strained part near the STI edges at the film surface (blue color), which arise due to elastically mechanical interactions within the structure to achieve a stress equilibrium [8]. For a certain ratio these two areas join in the middle of the film and cause a compressive strained surface above a tensile strained layer. For even larger ratios ($H/L > 2$) the strain relaxes almost fully and no compressive area arises. This is an unexpected behavior which needs more investigations from both experimental and simulation view point. However, for this work it is of minor relevance, since the devices studied next have an aspect ratio of about ~0.03 (active island length=2 µm, height=60 nm) and thereby suffer only marginally from stress relaxation (~5 %) due to STI formation.

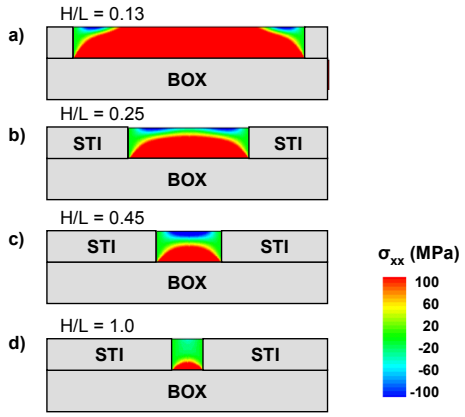

Fig. 8 Simulated stress distribution in patterned sSOI islands.

4.2 Electrical Results (Simulation & Experiment)

Threshold voltage measurements have been used to confirm the above hypothesis. In sSOI n-MOSFETs, there is a shift in the transistor threshold voltage ($\Delta V_{th}=V_{th,strained}-V_{th,unstrained}$) caused by strain-induced band modulation. The n-MOSFET long-channel threshold voltage was found to be around -100 mV lower than in unstrained SOI devices (in good agreement with other studies [1][9]). A comparison of the threshold voltage reduction combined with the data from Raman measurements and stress simulation results are shown in Fig. 9. Using the deformation potential theory with the parameters from [10], a threshold voltage reduction of ~200 mV would be expected for 1.3 GPa biaxial tensile stress. This is far from the experimentally observed 100 mV. By using instead the recently published values from [11], a much better agreement could be achieved. The threshold voltage shift demonstrates that the sSOI transistor channels are still fully strained after device processing.

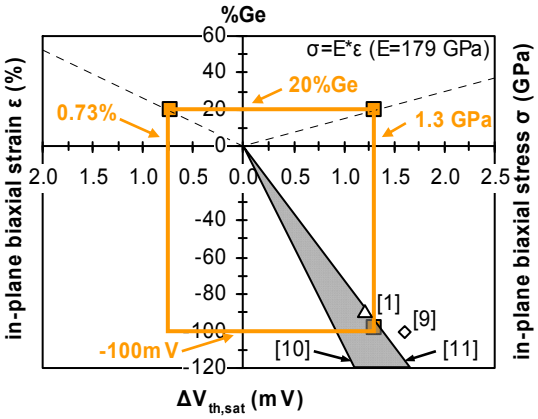

Fig. 9 Relation between strain, stress and threshold voltage shift for sSOI n-MOSFETs. The rectangle indicates measured and simulated data from this work.

The experimental gate length scaling of strained n-MOSFETs is investigated in Fig. 10. The linear and the saturation drain-current enhancement of sSOI devices with respect to unstrained SOI devices show a strong dependency on the gate length. For long

channel devices there is a substantially performance improvement (up to +80 %) which decreases as the gate lengths decrease.

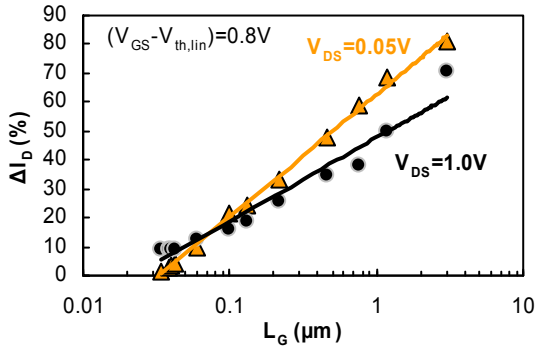

Fig. 10 Experimental drive current enhancements of sSOI devices compared to unstrained SOI devices vs. gate length.

As mentioned earlier, several effects could be involved. However, a lower coulomb mobility in sSOI devices seems unlikely, since the channel dopings are more or less the same for the strained and unstrained transistors. Also, stress relaxation seems not to be responsible as confirmed by mechanical simulations. The effect of approaching the saturation velocity is also not likely, otherwise the degradation should be worse for $\Delta I_{D,sat}$ than $\Delta I_{D,lin}$ in Fig. 10. The only remaining mechanism is parasitic $R_{S/D}$, which dominates the total resistance at short channel but not at long channel lengths, such that the impact of mobility gains will have less and less impact on drain currents as the gate length is scaled down.

Performing device simulations calibrated to unstrained SOI devices, a strong discrepancy between simulation and experiment exists (Fig. 11 blue curve). However, the general trend of reduced drain current gains with smaller gate lengths can be reproduced, and experimental data can be matched with an appropriate increase in parasitic $R_{S/D}$ used in the simulation.

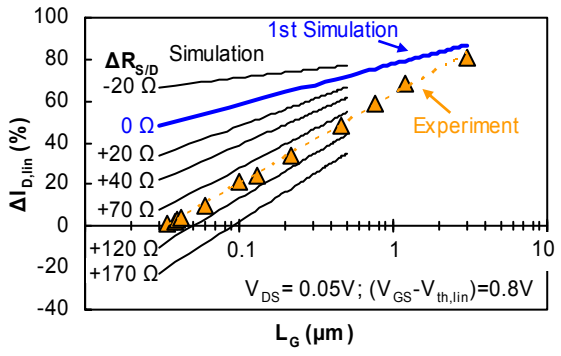

Fig. 11 Simulated linear drain current enhancement of sSOI devices in dependency of the gate length L_G for varying $R_{S/D}$ (experimental data is shown for comparison).

Measurement and extraction of the external resistance on sSOI vs. SOI wafers using the dR/dL-method shown in Fig. 12 reveals for the sSOI devices a ~130 Ω·µm higher $R_{S/D}$, despite a clearly higher mobility (lower slope) resulting from the biaxial tensile stress. This significantly higher $R_{S/D}$ roughly matches what the simulation in Fig. 11 predicts, and must be the cause for the more severe reduction of strain-induced benefits at shorter gate lengths, where the influence of $R_{S/D}$ on R_{total} is increased. The reasons for the higher $R_{S/D}$ on sSOI are not identified yet, but could be related to a poorer silicidation, an unoptimized process, or a higher defect density in the sSOI material.

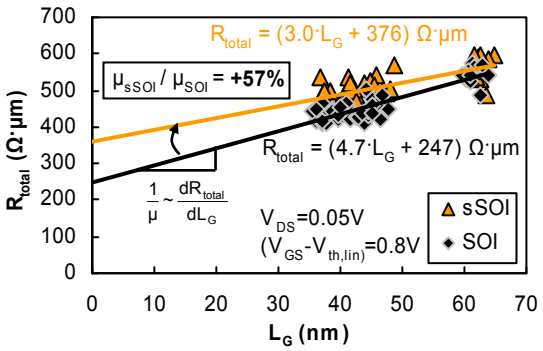

Fig. 12 n-MOSFET on-state resistance measurement at constant overdrive vs. L_G showing mobility improvement for sSOI but a ~130 Ω·µm higher parasitic source/drain resistance.

5. Conclusion

Measurements and simulations were performed to investigate the reduction of drive current benefits from biaxially strained SOI as the channel length is scaled. Mobility and threshold voltage measurements revealed that short channel sSOI transistors maintain the high mobility from the biaxial strain. Mechanical stress simulations showed the impact of STI formation on stress relaxation in biaxial tensile strained sSOI layers was dependent only on the aspect ratio of the resulting strained silicon island. However, for current state-of-the-art devices, these relaxation effects have only negligible influence, whereas a ~50 % higher parasitic source/drain resistance for sSOI devices was found to limit the stress-induced drive current enhancements in ultra-short channels.

Acknowledgments

This work was partially supported by the German Federal Ministry of Education and Research, and the French Ministry of Industry and MEDEA+ (DECISIF), registered under funding number 13N9880.

References

[1] A.V.Y. Thean *et al.*: Symp. VLSI Tech. Dig, pp. 134-135, 2005.
[2] K. Rim *et al.*: IEDM Tech. Dig., pp. 49, 2003.
[3] A. Wei *et al.*: ECS Trans. 6 (1), pp. 15-22, 2007.
[4] J.-S. Goo *et al.*: IEEE EDL, Vol. 24-5, pp. 351-353, 2003.
[5] D. Villanueva *et al.*: SISPAD 12-1, pp. 319-322, 2005.
[6] M. Horstmann *et al.*: IEDM Tech. Dig., pp. 233-236, 2005.
[7] B. Ghyselen *et al.*: Solid-State Electr. 48-8, p.1285-1296, 2004.
[8] S.C. Jain *et al.*: Phys. Rev. B (52)-9, pp. 6247-6253, 1995.
[9] H. Yin *et al.*: Symp. VLSI Tech. Dig, pp. 76-77, 2006.
[10] J. L. Egley: Solid-State Electr. 36, no. 12, p.1653-1664, 1993.
[11] J.-S. Lim *et al.*: Appl. Phys. Letters (89) 7, 073509, 2006.