Simulation and Optimization of Tri-Gates in a 22 nm Hybrid Tri-Gate/Planar Process

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***Abstract*: A Tri-Gate structure built into a planar 22 nm bulk process was investigated by 3-D device simulations (Sentaurus D-2010). The planar process flow sequence was extended with extra Tri-Gate patterning, but otherwise all implants were shared, as could be done in simultaneous processing of planar and Tri-Gate CMOS. A comparison of planar and Tri-Gate transistors with the same planar dopant profiles shows a substantial improvement of subthreshold slope, DIBL, and V_T-rolloff for Tri-Gates. The electrical behavior of the Tri-Gate transistor has been studied for various Tri-Gate heights and widths. A large space of Tri-Gate dimensions outperformed planar in terms of electrostatics and I_{ON}-I_{OFF} characteristics.**

I. INTRODUCTION

As scaling of CMOS transistors reaches the 22 nm node and beyond, even the most optimized planar MOSFETs suffer degraded electrostatic behavior at short channels [1]. For future scaling to the end of the ITRS roadmap, novel structures like FinFETs are required to improve electrostatic integrity of MOSFETs with gate lengths shorter than 20 nm [2-4]. Classical FinFETs with tall thin fins have a high aspect ratio which is difficult to implement into existing planar process flows. A Tri-Gate transistor with low-profile fins has the advantage of being more compatible with existing planar process flows. It is even possible to produce Tri-Gates in parallel to planar MOSFETs [5], where Tri-Gates would be used in high speed logic and low minimum voltage circuitry, and planar would be used for longer channel applications such as analog and I/O. This Tri-Gate/planar hybrid concept allows design portability into a 3-D CMOS technology, which is very important for SoC time to market.

Ideally, a Tri-Gate process flow could even be run without any additional masking, by sharing implants and metal gate workfunction metals with planar transistors. This work uses 3-D simulations to study the electrical behavior of Tri-Gates built into a bulk planar process. Tri-Gates are patterned and implanted with planar wells, extensions, and halos, as well as insitu-doped epitaxial S/Ds from a planar process. Dual band-edge metal gate workfunctions from a planar process are also used in the Tri-Gate structures. The resulting Tri-Gate built into a planar process shows excellent improvement in electrostatic behavior compared to a planar transistor for the same process sequence. The improved electrostatic behavior of the Tri-Gate allows scaling of L_{gate} with less drive current and V_T mismatch degradation compared to planar.

II. DEVICE STRUCTURE

A planar CMOS process was first simulated in 3-D around 22 nm technology ground rules with an assumed nominal L_{gate} = 26 nm and $T_{ox,inv}$ = 1.0 nm, in line with ITRS assumptions. Extension, halo, epitaxial S/D, and anneal conditions were tuned for good electrical integrity, with I_{OFF} = 40 nA/µm and a subthreshold slope ca. 90 mV/dec. This study focuses on the NMOS results only, since similar trends apply to PMOS.

Additional steps were then added to the 3-D planar process simulation to create a Tri-Gate structure, as shown in Fig. 1. After Tri-Gate formation, it is assumed that a planar FET and Tri-Gate would run the identical process.

- STI
- Well implants
- Tri-Gate and dummy gate patterning
- S/D extension and halo implants
- eSiGe module
- NMOS raised S/D module
- Activation anneal
- Replacement gate
- Silicidation and contacts

Fig. 1: *Process sequence of 22 nm bulk transistor*

Fig. 2 illustrates an NMOS Tri-Gate transistor (cut at the half Tri-Gate width to reduce simulation time) after the process simulation. Because the implants and epitaxial S/D are identical to that of the planar MOSFET, the resulting dopant profiles in the Tri-Gate transistor are nearly identical to that of the planar process.

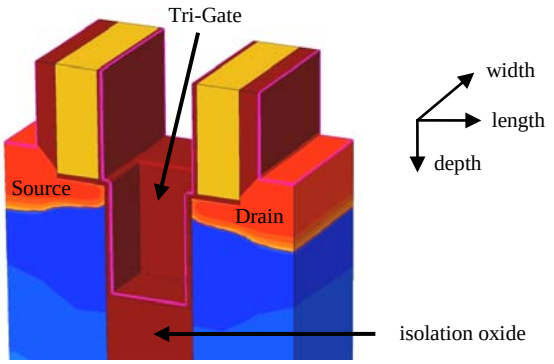

Fig. 2: *Simulated n-Tri-Gate transistor cut at the half Tri-Gate transistor width.*

III. Results and Discussion

A. Comparison between Tri-Gate and planar transistor

For the comparison we simulated a planar and a Tri-Gate NMOS with a total structure width of 50 nm and a nominal gate length of 26 nm. The Tri-Gate width was set to 25 nm and the fin height to 20 nm. Fig. 3 shows the transfer characteristics of planar vs. Tri-Gate for the linear and saturated regimes. Due to a low rapid temperature and a laser anneal, the planar transistor already has a good subthreshold slope of 90 mV/dec and DIBL of 97 mV/V. The Tri-Gate transistor with the side gates has significantly better gate control with a steeper subthreshold slope of 72 mV/dec and much smaller DIBL of 49 mV/V.

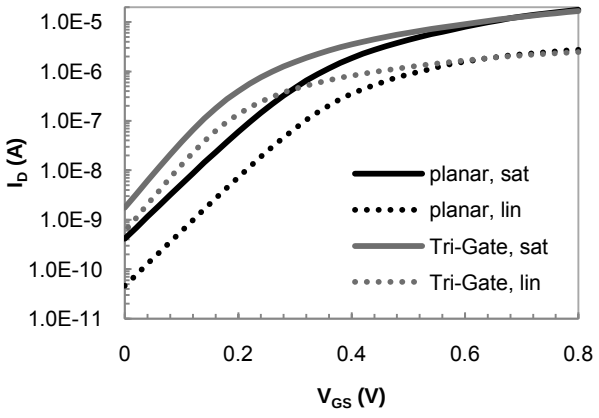

Fig.3: *Transfer characteristic (log.) for a planar and Tri-Gate transistor*

The significance of the enhanced electrostatic behavior of the Tri-Gate is illustrated in Fig. 4. While the planar FET has significant $V_{T,sat}$ rolloff to subnominal, the Tri-Gate rolloff curve remains relatively flat.

Note that in this study, we compare Tri-Gate vs. planar from an optimized planar FET implant starting point. With an optimized planar FET starting point, the Tri-Gate exhibits enhanced reverse short channel effects and higher leakage due to corner effects [7]. For an enhancement-mode transistor with V_{DS} = 0.8 V there is already a high electron density at the corners of the Tri-Gate (Fig. 5). But in a true Tri-Gate/planar hybrid technology, the dopant profiles would be optimized for the Tri-Gate with lower reverse short channel effect and to supress corner effects. The planar FETs would run at longer channel lengths out of the critical speed paths where the modified halos and wells would not make a significant impact. In addition, due to the corner rounding inherent in FEOL cleaning, it is expected that the corner leakage effect will be effectively supressed, as reported in [8-9].

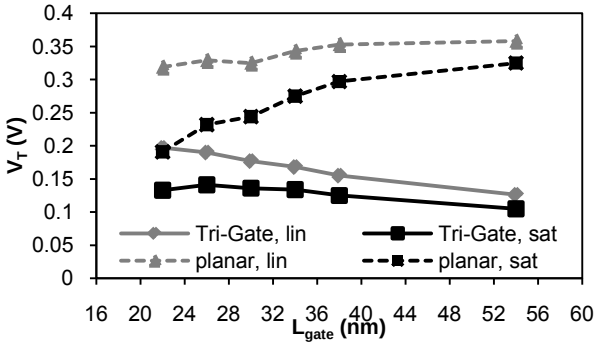

Fig.4: *Simulated roll-off curve for a planar and Tri-Gate transistor*

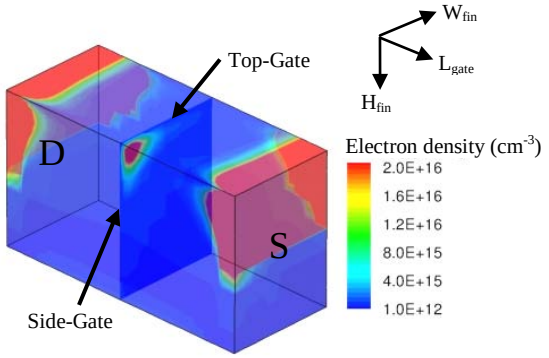

Fig.5: *Simulated electron density for a n-Tri-Gate transistor cut at the half transistor width (V_{GS} = 0 V, V_{DS} = 0.8 V)*

B. Variation of Tri-Gate height and width

Clearly the Tri-Gate width and height dimensions relative to the planar doping profiles are critical to electrostatics and drive current per drawn width. Too wide and too short the Tri-Gate becomes planar-like. Too tall and too narrow the structure becomes resistance dominated since the planar FET extensions used are

shallow in nature. To study these sensitivities, different heights and widths of the Tri-Gtaes were simulated at nominal gate length.

Fig. 6 shows the I_{OFF} vs. I_{ON} behavior for Tri-Gate heights between 5 and 25 nm in 5nm increments, and Tri-Gate widths between 20 and 35 nm. Note that each point represents a unique set of Tri-Gate width and height at nominal gate length and for the same implant conditions. I_{OFF} and I_{ON} are normalized to effective Tri-Gate width equal to 2*height + width for each Tri-Gate. For NMOS transistors with smaller Tri-Gate width, the drive current improves. That is the same behavior as classical FinFET with a high aspect ratio [6]. But the variation of the fin height shows that performance becomes worse for Tri-Gates with a higher fin over H_{fin} = 7 nm because the side gate area increases without a direct connection to the source drain regions, where extension junction depth is ca. 7nm.

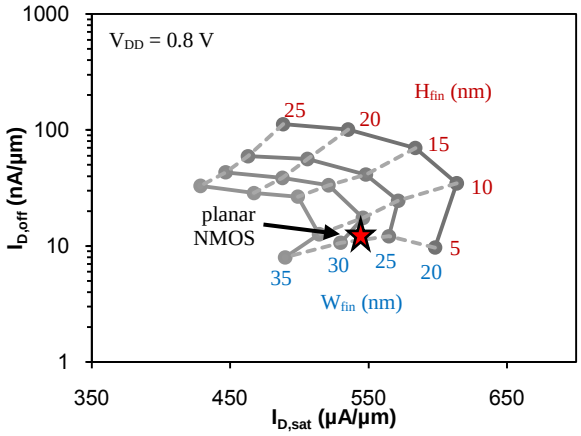

Fig. 6: *$I_{D,off}$ to $I_{D,sat}$ normalized to total gate width for different widths and heights of Tri-Gate (L_{gate} = 26 nm).*

A similar representation of H/W ratio is seen in Fig. 7. Starting with a planar transistor which has a high ratio of $I_{D,sat}$ to $I_{D,off}$ (ca. $4*10^5$) the performance of the transistor decreases very fast with an increasing fin height. The corner effect becomes stronger and supports the leakage current more than the drive current.

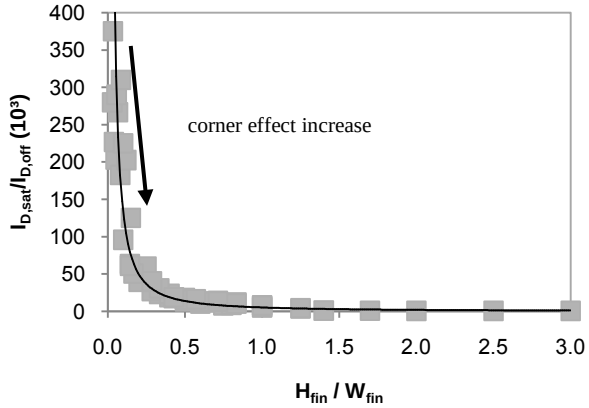

Fig. 7: *$I_{D,sat}$ / $I_{D,off}$ ratio as a function of fin height / fin width (L_{gate} = 26 nm).*

The simulated behavior can be described by the empirical equation (1). Thus for performance, it is critical to control the Tri-Gate height dimension.

$$\frac{I_{D,sat}}{I_{D,off}} = 5.2 * \left(\frac{H_{Tri-Gate}}{W_{Tri-Gate}}\right)^{-1.4} \qquad (1)$$

Electrostatics are not as sensitive to the height to width ratio and shows a stable behavior with ca. 73 mV/dec over a larger region of the ratio (Fig. 8). For transistors with a small and wide fin, the slope approaches the value of the planar NMOS (90 mV/dec). The subthreshold slope increases for transistors with a higher fin than 25 nm because the side gates reach a depth of the substrate where the channel doping becomes weaker and the gate control is degraded.

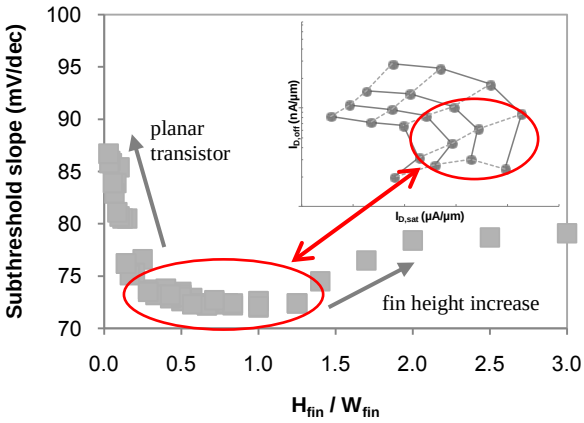

Fig. 8: *Subthreshold slope as a function of Tri-Gate height to Tri-Gate width with an optimal regime of 0.6-1.3 (L_{gate} = 26 nm).*

The $I_{D,sat}/I_{D,off}$ ratio and the subthreshold slope of the n-Tri-Gate transistor shows an optimum for a Tri-Gate height between 5 and 10 nm and the smallest simulated Tri-Gate width with 20 nm. Note the large space of Tri-Gate dimensions which outperform planar in terms of I_{ON}-I_{OFF} as well as subthreshold slope, as circled in Fig. 8.

IV. Conclusion

A Tri-Gate approach with a planar process starting point has been evaluated for 22 nm ITRS technology assumptions. Such an approach is the basis for a low-cost Tri-Gate/planar hybrid technology, where Tri-Gates and planar would share the same implant masking, same S/D processes, and same dual band-edge metal gate workfunctions. 3-D simulations show that Tri-Gate NMOS have significantly better electrostatics and I_{ON}-I_{OFF} performance compared to a planar NMOS with the same dopant profiles and gate oxide thickness. It has been demonstrated that there is a large design space of Tri-Gate dimensions with superior performance

compared to planar.

The performance benefit of Tri-Gates and the cost benefits of sharing implants between Tri-Gates and longer channel planar FETs are clear. However, this approach is very sensitive to the height of the Tri-Gate. The Tri-Gate height must be very well controlled in the process. SOI substrates offer the possibility of good Tri-Gate height control, but potentially pays a performance penalty due to the limited silicon volume available for embedded stressors such as S/D SMT and embedded-SiGe. Thus the challenge to manufacturing is to control the Tri-Gate height on a bulk substrate, where full embedded stress benefits can be realized [11-12].

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