An Approach for Small-Signal Models for RF on CMOS Application with Consideration of Substrate Influence

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ABSTRACT

Utilizing a tuned 2D/3D simulation, a physics based small signal model including the substrate effect is proposed for accurately predicting the RF performance of 0.35μm Standard CMOS devices. The calculation is based on the drift diffusion model and specifically by using of Mock's procedure. With the aid of postprocessing the small signal behavior was determined and the equivalent circuit elements of the intrinsic and the parasitic part of the MOSFET were calculated. The calculated data and elements of the equivalent circuit model are computed in the range from 1GHz to 100GHz. The data shows the transformation of the MOSFET from an active element to a passive element.

Keywords: *physical device simulation, semiconductor device modeling, RF-CMOS parasitics*

1. Introduction

The growing market of communication products demands low cost circuits. That is why the microelectronics industry is concentrating on the design and development of systems that include the digital baseband subsystem and the analog/RF front-end in a single chip.

Advances in CMOS process technology have continued to reduce the minimum channel length of the MOS device, consequently increasing the unity gain cut off frequency, f_T, of the transistors. Now f_T's exceed 100GHz [1]. The focal point is put on CMOS technology due to its low cost compared to its bipolar counterpart. CMOS technology allows to unite the issues of RF analog and baseband digital circuit integration in the same silicon chip. The most critical part of such a system is the RF front-end which mainly defines the quality of received/transmitted signals. The design of monolithic RF-CMOS circuits has been the subject of recent research efforts [2]-[6]. A handicap for the realization of commercial RF components in a standard CMOS technology is the lack of models that accurately predict the MOS device behavior at high frequencies and also consider the influence at the substrate. The small-signal equivalent circuit model for the intrinsic Si MOSFET with contact and wire parasitics is already described [7, 8] and the investigation of the substrate influence has begun [9]-[11].

Layout differences between simple MOS and RF MOS transistors cause modifications of bulk effects. With the method of Kolding [12] to include bulk straps and to divide a RF transistor into clusters, it may be possible to obtain scalable RF CMOS models.

Contemporary models are based upon accurate parameter extraction approaches including S-parameter measurements and Y-parameter analysis. This implies the realization of a plurality of test structures together with a proper de-embedding method. A faster way to obtain these elements is with a physical device simulation using a tuned simulator.

During the last years, computer performance has risen to a level where 3D simulation of sub-micron elements is more effective [13, 14].

This paper describes a method to determine the resistances between source/drain junctions and the substrate contacts using a 2D/3D dimensional simulator.

2. The Simulator

For our simulations we used the 2D/3D numerical simulator SIMBA [15, 16] SIMBA is based on two and three-dimensional solutions of the Poisson equa-

tion

$$\nabla \cdot (\epsilon \nabla \varphi) = -e \left(p - n + N_D^+ - N_A^- \right) \tag{1}$$

(N_D^+, N_A^- are the ionized donor and acceptor densities),
the continuity equations for holes and electrons:

$$\nabla \cdot \mathbf{J}_p = -e \left(R - G + \frac{\partial p}{\partial t} \right) \tag{2}$$

$$\nabla \cdot \mathbf{J}_n = e \left(R - G + \frac{\partial n}{\partial t} \right) \tag{3}$$

($\mathbf{J}$: current density, R: recombination rate, G: generation rate)
and the corresponding transport equations

$$\mathbf{J}_p = -e\mu_p p \nabla \varphi - kT\mu_p \nabla p \tag{4}$$

$$\mathbf{J}_n = -e\mu_n n \nabla \varphi - kT\mu_n \nabla n \tag{5}$$

(μ_p, μ_n hole and electron mobility).

The dynamic simulation is done by using Mock's procedure [17]. For a final comparison with known data we compared the calculated transit frequencies (f_T) and the maximum frequency of oscillation (f_{max}) with data taken from measurement. At a certain bias point, a voltage step is applied to the gate and the transit behavior is calculated, until the stationairy solution is reached. Then the output transient is generated in the same way. We computed the complex conductance parameters as follow:

$$\begin{aligned} &\Re\left\{\mathbf{y}^{i+1}(\omega)\right\} = \\ &\quad \Re\left\{\mathbf{y}^{i}(\omega)\right\} + \frac{\Delta I^i}{\Delta U}\left[\cos\left(\omega T^i\right) \cdot \frac{\sin\left(\omega \Delta t^i\right)}{\omega \Delta t^i}\right. \\ &\quad \left. + \sin\left(\omega T^i\right) \cdot \frac{\cos\left(\omega \Delta t^i\right) - 1}{\omega \Delta t^i}\right] \end{aligned} \tag{6}$$

$$\begin{aligned} &\Im\left\{\mathbf{y}^{i+1}(\omega)\right\} = \\ &\quad \Im\left\{\mathbf{y}^{i}(\omega)\right\} - \frac{\Delta I^i}{\Delta U}\left[\sin\left(\omega T^i\right) \cdot \frac{\sin\left(\omega \Delta t^i\right)}{\omega \Delta t^i}\right. \\ &\quad \left. - \cos\left(\omega T^i\right) \cdot \frac{\cos\left(\omega \Delta t^i\right) - 1}{\omega \Delta t^i}\right] \end{aligned} \tag{7}$$

On the basis of these elements the current gain h_{21}, the maximum available gain (MAG) and the maximum stable gain (MSG) can be calculated [18]:

$$h_{21} = \left| \frac{\mathbf{y}_{21}}{\mathbf{y}_{11}} \right| \tag{8}$$

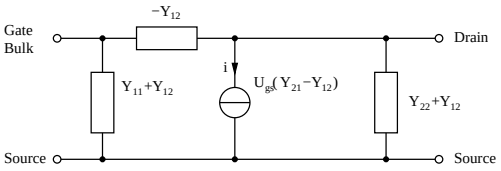

Fig. 1. π-elements of the conductance matrices

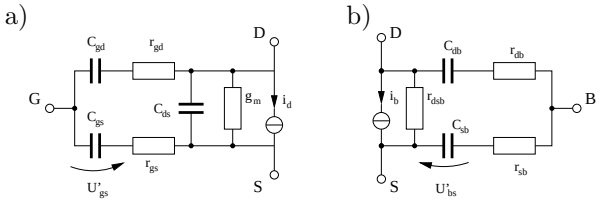

Fig. 2. Equivalent circuit elements

$$\text{MSG} = \left| \frac{\mathbf{y}_{21}}{\mathbf{y}_{12}} \right| \tag{9}$$

$$\text{MAG} = \left| \frac{\mathbf{y}_{21}}{\mathbf{y}_{12}} \right| \cdot \left(k - \sqrt{k^2 - 1} \right)$$

$$k = \frac{2\Re\{\mathbf{y}_{11}\}\Re\{\mathbf{y}_{22}\} - \Re\{\mathbf{y}_{12}\}\Re\{\mathbf{y}_{21}\}}{|\mathbf{y}_{22}\,\mathbf{y}_{21}|} \tag{10}$$

Fig 1 shows the relationship between the conductance matrix elements and the equivalent circuit elements. The comparison of the elements of the intrinsic MOSFET and the conductance matrices shows the dependency of the two schematics. To get the small signal elements we split the real and imaginary part of the complex conductances. Fig. 2 shows such a schematic. The current of the voltage controlled sources are calculated as follows:

$$i_d = U'_{gs}\, g_m\, e^{-\jmath\omega\tau_1} \tag{11}$$

$$i_b = U'_{bs}\, g_{mb}\, e^{-\jmath\omega\tau_2} \tag{12}$$

The determination of the parasitic elements is similar to the determination of the intrinsic elements.

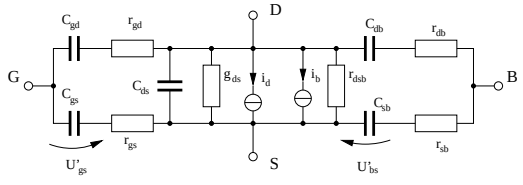

Fig. 3. Combined equivalent circuit elements

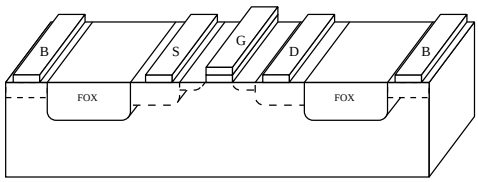

Fig. 4. Used MOSFET structure

For the calculation of the intrinsic elements, the substrate contact (B) was clamped to $V_{bs} = 0V$. To get the parasitic elements, we clamped the gate contact to a certain bias point and applied the input transient to the substrate contact. The comparison between the intrinsic and parasitic elements of the MOSFET shows great similarity. With this assumption it is possible to calculate the parasitic elements in the same way. The elements between drain and source are in this case negligible compared to the intrinsic parameters.

Under the condition that the bias points of the source and drain contacts in both simulations are the same, we can combine the two equivalent circuits. The result is shown in Fig. 3

3. Simulation and Results

For our investigation we have chosen a 0.35μm CMOS mixed signal technology. We used transistors with a gate width of 20μm and a separate substrate connection similar to the cross section shown in Fig 4.

The general basis of our investigations include doping profiles from a technology simulator and also

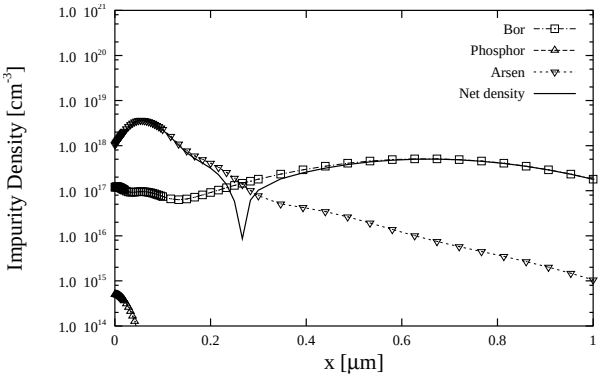

Fig. 5. Impurity densities of the n-channel-LDD regions

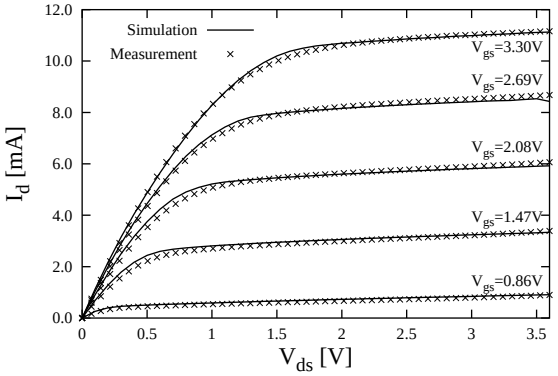

Fig. 6. Output characteristics n-MOSFET

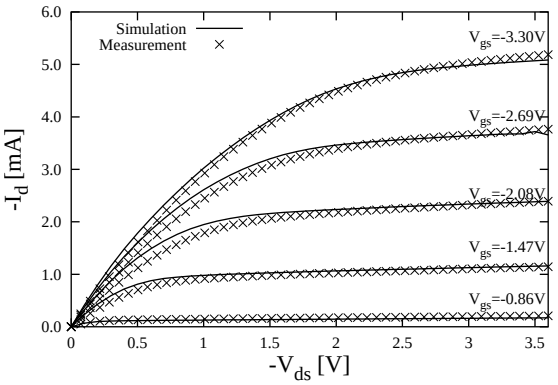

Fig. 7. Output characteristics p-MOSFET

	r_{gs} [Ω]	C_{gs} [fF]	r_{gd} [Ω]	C_{gd} [fF]
n	64	20	≈ 0	2.3
p	165	17	≈ 0	2.3
	C_{ds} [fF]	g_d [mS]	g_m [mS]	τ [ps]
n	16	0.22	4.3	1.33
p	9.3	0.15	2.0	2.0
	r_{bs} [Ω]	C_{bs} [pF]	r_{bd} [Ω]	C_{bd} [pF]
n	94	30	144	16
p	83	13	72	6

Table 1. Equivalent circuit elements, valid up to 10GHz

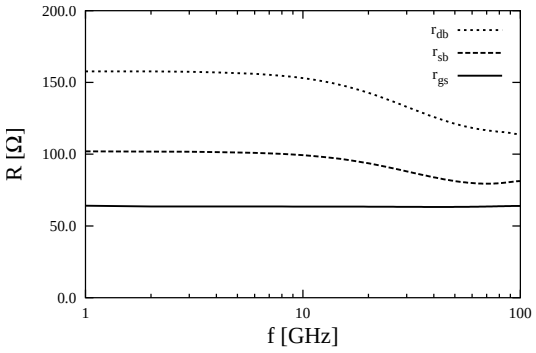

Fig. 8. Resistors for the equivalent circuit at $V_{gs} = 2\text{V}$ and $V_{ds} = 3\text{V}$

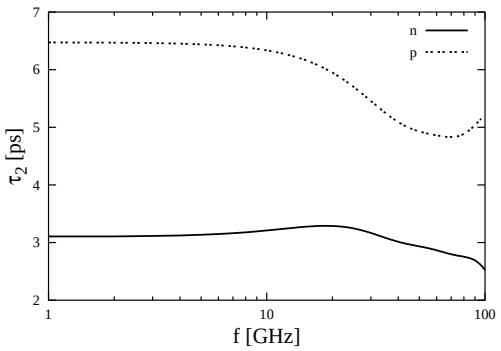

Fig. 10. Time delay of the substrate source at $V_{gs} = 2\text{V}$ and $V_{ds} = 3\text{V}$

lab measurements. For describing the doping profile within our simulation we used the Gaussian distribution for ion implantations [19]. The generated doping profiles (Fig. 5) were compared with the data from the process simulation and with additional measurements.

For adjusting the simulator to the technology, the transfer and output characteristics are computed and compared with measurements. The results of this static analysis are shown in Fig. 6 and 7.

We also calculated and measured the frequency characteristics. For the n-MOSFET we got in both cases a f_T of 32GHz and a f_{max} of 48GHz. The calculated results for the p-MOSFET are $f_T = 17\text{GHz}$ and $f_{max} = 38\text{GHz}$ This step was included to verify the frequency behavior of the MOSFETs. After the verification of the model, we calculated the equivalent circuit elements. As an example of the results of the frequency calculation, the resistors of the intrinsic and parasitic part are included (Fig. 8). This figure shows good linearity in the area below 10GHz. The other linear equivalent circuit elements in these area are listed in table 1.

The influence of the current source is small. As shown in Fig. 9, the control factor is about 10 times lower then the control factor of the voltage controlled source of the gate. This means, the current through the MOSFET is mainly defined by the voltage controlled current source of the gate. Additionally, the time delay (shown in Fig. 10) is much larger than the time delay of the gate current source.

Not negligible is the substrate resistance r_{dsb}. As shown in Fig. 11, the resistance of the n-MOSFET shows no valid data above 10GHz. Below this border the resistance is at least twice higher than the equivalent source drain resistance in the gate sector. The frequency behavior of the r_{dsb}-resistance limits

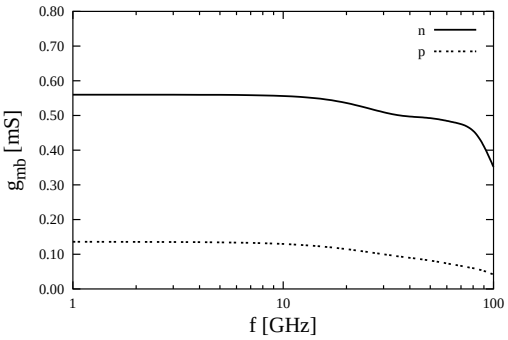

Fig. 9. Forward transconductance of the substrate source at $V_{gs} = 2\text{V}$ and $V_{ds} = 3\text{V}$

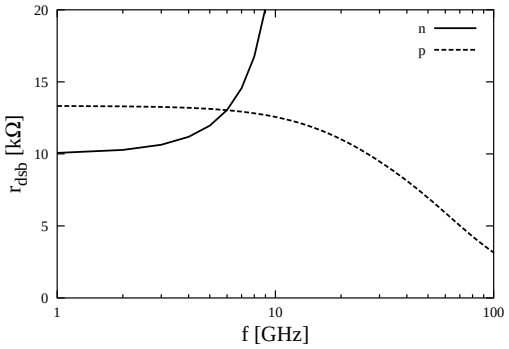

Fig. 11. Substrate resistance vs. frequency at $V_{gs} = 2\text{V}$ and $V_{ds} = 3\text{V}$

the equivalent circuit model for the n-MOSFET up to 5GHZ. The model of the p-MOSFET is valid at least to 10GHz.

Further investigations should take a look at the resistor r_{dsb}. It shows a strong influence on the channel conductance.

4. Conclusion

Numerical simulations of n- and p-channel MOS transistors have been used to predict the high frequency behavior of such devices in a 0.35μm mixed signal CMOS technology. The simulator was tuned by utilizing static FET characteristics. A small signal model considering the substrate effect is proposed. The predicted transit frequency for n- and p-MOSFETs exhibit a good agreement with measurements.

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