Optimization of Nano-Scaled Implantation Free InGaAs MOSFETs

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Abstract
The influence of structure parameters of implantation free InGaAs MOSFETs on the static and dynamic transistor behavior was simulated by a quantum hydrodynamic model calibrated by experimental results from a 1 µm transistor. Structures with gate lengths from 100 nm to 25 nm were investigated. For the state-of-the-art gate length of 50 nm, cut-off frequencies f_t = 230 GHz and f_{max} = 350 GHz were calculated.

Keywords: InGaAs MOSFET, enhancement mode, simulation, quantum hydrodynamic model.

1. INTRODUCTION

Due to the higher electron mobility in GaAs and other III-V compound semiconductor materials, GaAs-based devices like MESFETs and HEMTs are widely used for high speed circuit applications and monolithic microwave integrated circuits. However, the gate current of the Schottky contact increases strongly at forward biased gate contacts. Therefore enhancement-mode MESFETs or HEMTs are strongly limited in their control voltage swing. In contrast, GaAs-based MOSFETs enable larger gate voltages and have also higher input impedances. Hence low-power circuits with high-speed operation can be combined with high packing density.
In [1], [2], [3] an enhancement-mode n-channel MOSFET was presented with an amorphous Ga_2O_3/GdGaO dielectric ($\kappa \cong 20$), a gate length of 1 µm and an $In_{0.3}Ga_{0.7}As$ channel. Based on the experimental results, the model parameters of a quantum hydrodynamic transport model [4], which is implemented in our 2D/3D-numerical device simulation program SIMBA [5], are calibrated. Thereafter the structure was scaled for gate lengths of 100 nm, 50 nm and 25 nm, respectively. Static and dynamic device simulation results are I-V characteristics, transconductances as well as cut-off frequencies.

2. SIMULATION MODELS

Quantum hydrodynamic (QHD) models, which are based on a quantum fluid dynamic model, offer new ways to understand and design quantum sized semiconductor devices. The advantage of this model is its macroscopic character, which enables to obtain a description without knowing of quantum mechanical details like the initial wave function [6]. The classical hydrodynamic (HD) model for semiconductor device simulation can be extended by further terms in the transport equations and in the energy balance equations. They describe an internal quantum potential in the transport equation as well as a quantum heat flux in the energy balance equation. These additional terms in the classical hydrodynamic model allow to describe the continuous electron and hole distribution in a semiconductor device, accumulations of carriers in potential wells and resonant tunneling of carriers, respectively. The standard model for universal device simulations is the drift-diffusion (DD) model, which can be derived from the above mentioned model.

Basic equations of the QHD model are the Poisson equation, continuity equations, transport equations, energy balance equations, energy flux density equations and equations for the quantum correction potential. Further approaches are necessary for carrier mobilities, generation and recombination rates, diffusion coefficients and energy relaxation times, which are almost material dependent. Solutions of the equations are achieved by a successive algorithm (the so called Gummel algorithm). For solving the partial differential equations a box method is used. The resulting non-linear equation systems are solved by the NEWTON-method and the corresponding linear equation systems by preconditioned gradient methods. All models are implemented fully three-dimensionally in the SIMBA program system [4], [5].

3. BASIC STRUCTURE SIMULATION AND VERIFICATION

The starting point for the simulations is the basic structure represented in Fig. 1, as a functionally relevant detail of the real device, published in [3].

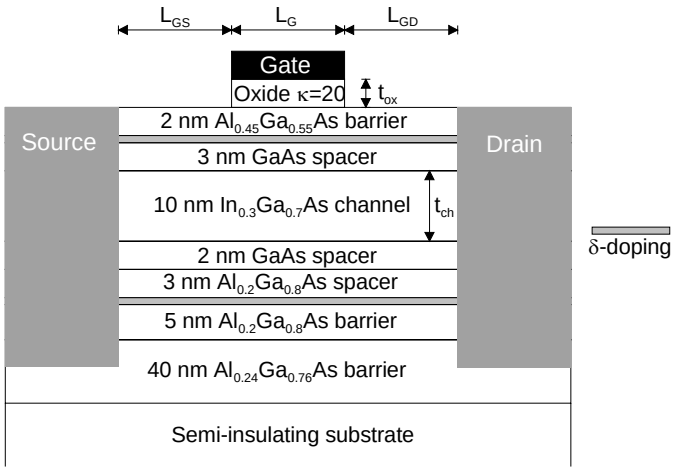

Fig. 1. Basic structure for the simulations [3]

The different structure parameters are gate length as well as gate-to-source and gate-to-drain distance $L_G = L_{GS} = L_{GD}$ = 1 µm, gate oxide thickness t_{ox} = 17 nm, top delta doping $N_{st} = 0.6 \cdot 10^{12}$ cm^{-2} and bottom delta doping $N_{sb} = 1.8 \cdot 10^{12}$ cm^{-2}. All other layers are undoped. The dielectric gate stack consists of $Ga_2O_3/(Gd_{0.6}Ga_{0.4})_2O_3$ with a dielectric constant κ = 20 [3]. Fig. 2 shows the calculated transfer characteristic and the transconductance in comparison to experimental results from [3]. The simulation of the small-signal behavior results in a transit frequency f_t = 12 GHz and a maximum frequency of oscillation f_{max} = 32 GHz (Fig. 2).

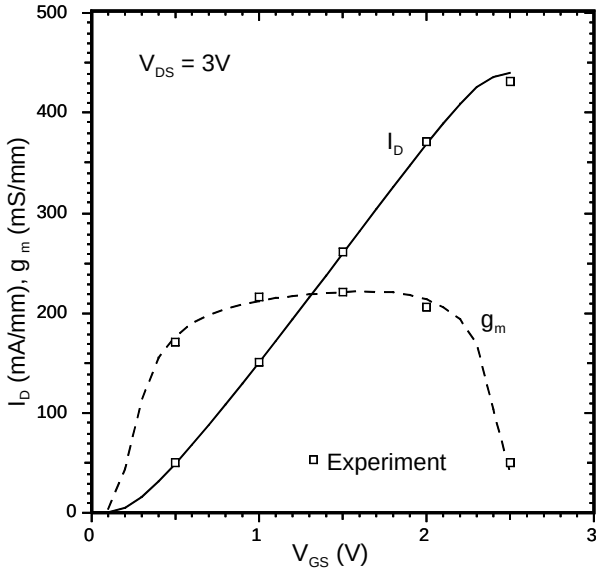

Fig. 2. Transfer characteristic and transconductance - simulation and experiment [3]

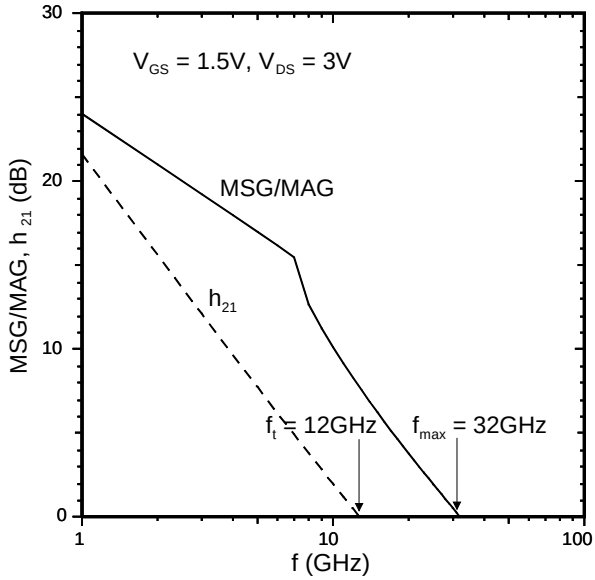

Fig. 3. Calculated small-signal gains

4. PARAMETER VARIATIONS

In the following, the structure (Fig. 1) was scaled for gate lengths of 100 nm, 50 nm and 25 nm, respectively. The layer structure for different gate lengths [L_G = 100 nm / 50 nm / 25 nm] consists of a 40 nm undoped $Al_{0.24}Ga_{0.76}As$ layer, a 5 nm $Al_{0.2}Ga_{0.8}As$ barrier layer, a bottom Si δ-doping, a [2 nm / 1.5 nm / 1 nm] $Al_{0.2}Ga_{0.8}As$ spacer layer, a [2 nm / 1.5 nm / 1 nm] GaAs spacer layer, a [t_{ch} = 10 nm / 5nm / 4 nm] undoped $In_{0.3}Ga_{0.7}As$ channel layer, a [2 nm / 1.5 nm / 1 nm] GaAs spacer layer, a top Si δ-doping, a [2 nm / 1.5 nm / 1 nm] $Al_{0.45}Ga_{0.55}As$ barrier layer and a t_{ox} = 4 nm Ga_2O_3/GdGaO dielectric stack. Furthermore $L_{GS} = L_{GD} = L_G$ was assumed for all structures. The threshold voltage was

adjusted with two equal δ-dopings [$2{\cdot}10^{12}$ cm^{-2} / $3{\cdot}10^{12}$ cm^{-2} / $3.2{\cdot}10^{12}$ cm^{-2}] to V_{th} = 0.1 V at V_{DS} = 2V. Only at L_G = 25 nm, a reduction of gate oxide was not avertable for further improvements, hence t_{ox} = 2 nm was fixed as a lower limit.
The calculated transfer characteristics and the transconductance for separate gate lengths are represented in Fig. 4. Fig. 5 shows the cut-off frequencies f_t and f_{max} at V_{DS} = 2 V and V_{GS} at the maximum transconductance value. At L_G = 25 nm, a maximum transconductance of 1510 mS/mm and cut-off frequencies f_t = 300 GHz and f_{max} = 380 GHz can be achieved.

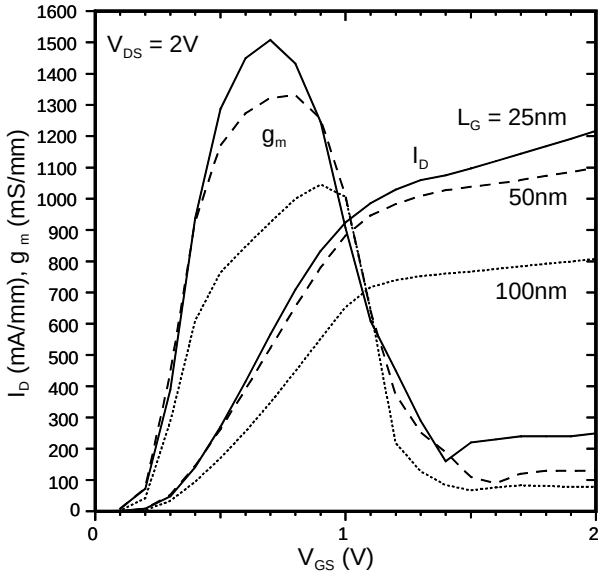

Fig. 4. Transfer characteristics and transconductance for different gate lengths

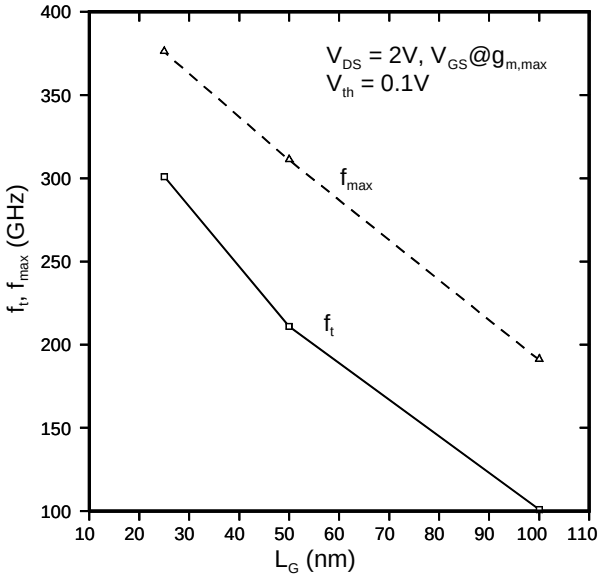

Fig. 5. Cut-off frequencies for different gate lengths

For the state-of-the-art gate length of 50 nm further simulations have been carried out. The channel thickness t_{ch} was varied in the range of 4 nm to 8 nm. The threshold voltage was adjusted to V_{th} = 0.1 V by adapted δ-dopings. The resulting maximum drain current and transconductance at V_{GS} = V_{DS} = 2V are depicted in Fig. 6 and the corresponding cut-off frequencies in Fig. 7. Smaller channels lead in connection with higher δ-dopings to increasing currents and transconductance and consequently to increasing cut-off frequencies.

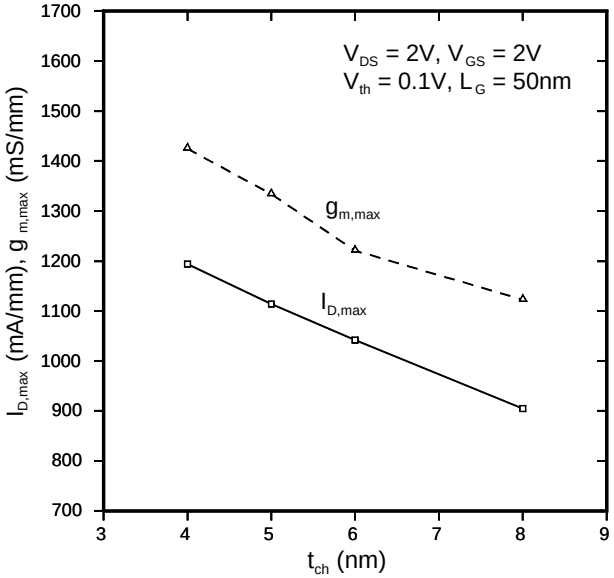

Fig. 6. Maximum drain current and transconductance for different channel thickness

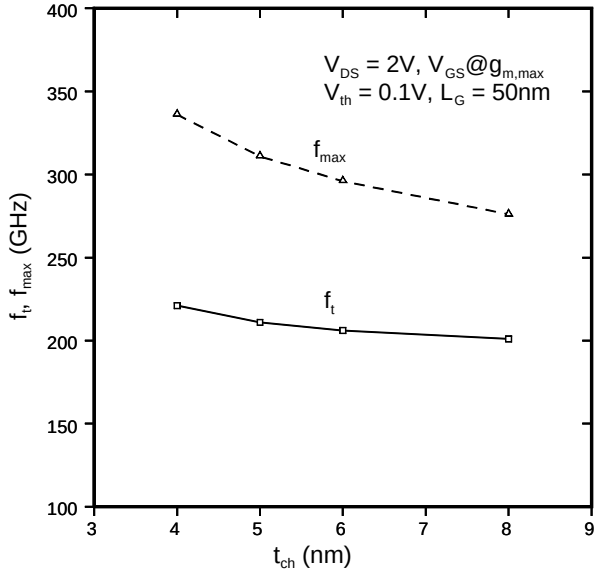

Fig. 7. Cut-off frequencies for different channel thickness

The results of oxide thickness variation are represented in Fig. 8 and Fig. 9. Thin oxides allow higher dopings at the same threshold voltage and thus higher drain currents and transconductances. Reduced oxide thickness causes a rising gate capacity and therefore the increasing transconductance results only in a moderate increment of cut-off frequencies. A structure with L_G = 50 nm and t_{ch} = 4 nm as well as t_{ox} = 2 nm achieves $g_{m,max}$ = 1730 mS/mm, f_t = 230 GHz and f_{max} = 350 GHz.

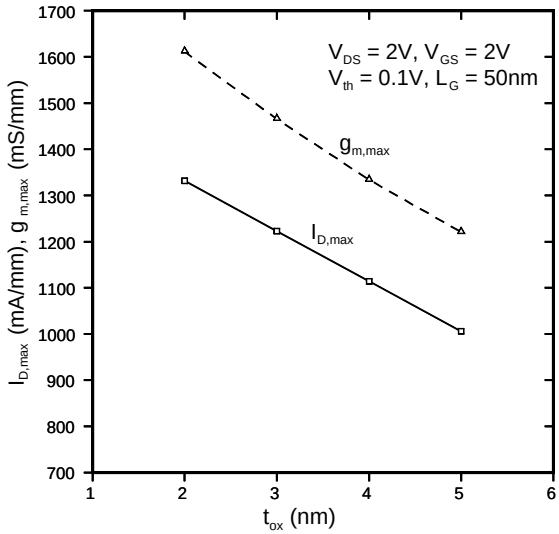

Fig. 8. Maximum drain current and transconductance for different gate oxide thickness

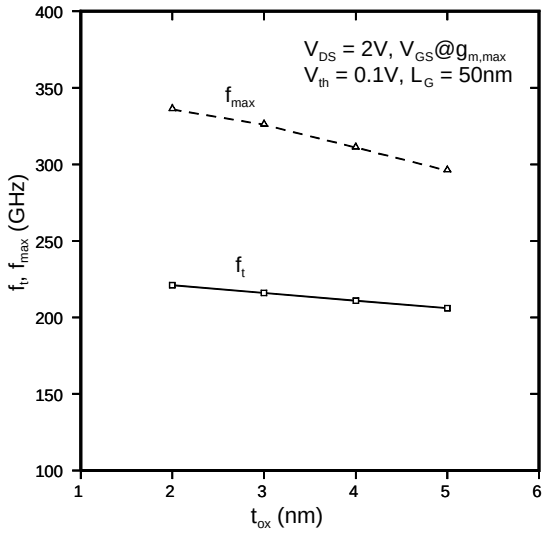

Fig. 9. Cut-off frequencies for different gate oxide thickness

5. CONCLUSIONS

Numerical simulations of nano-scaled implantation free InGaAs MOSFETs have been carried out by a quantum hydrodynamic model. After model parameter calibration by experimental results the structure was scaled down to 25 nm gate length. Structure parameter variations are carried out for the state-of-the-art gate length of 50 nm. In this case cut-off frequencies of f_t = 230 GHz and f_{max} = 350 GHz can be reached.

6. REFERENCES

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